

# Towards axial Si/GaAs nanowire heterostructures

D. Beznasiuk<sup>1</sup>, P. Gentile<sup>2</sup>, G. Claudon<sup>1</sup>, M. Hocevar<sup>1</sup>

<sup>1</sup> Institut Néel CNRS/UJF UPR2940, 25 rue des Martyrs, 38042 Grenoble, France

<sup>2</sup> CEA Grenoble, INAC-SP2M-SINAPS, 17 rue des Martyrs, 38054 Grenoble, France

daria.beznasiuk@cea.fr

III-V/Si semiconductor heterostructure nanowires are a promising strategy to integrate light emitters on Si. Indeed, the small nanowire cross-section allows to elastically release strain on the lateral walls of the nanowires, preventing the formation of misfit dislocations. For example, GaAs/Si has a lattice mismatch of 4%. Such structures can be created in axial heterostructure nanowires with diameters up to 80 nm [1], whereas such high lattice mismatch is detrimental in two dimensional GaAs epitaxy on Si [2,3]. Based on these theoretical assumptions, we fabricated GaAs/Si axial heterostructure nanowires and studied their structural properties using transmission electron microscopy.

The Si nanowires were grown on Si (111) substrates by the vapor-liquid-solid mechanism using Au colloids in a chemical vapor deposition reactor. Then, we transferred the Si nanowire samples to the molecular beam epitaxy (MBE) reactor to grow the GaAs segment. As the samples were exposed to air between the growth sequences, we treated the Si nanowires to remove the native SiO<sub>2</sub> just before the introduction to the MBE chamber. Different chemical solutions were tested to remove the native oxide including hydrofluoric acid and buffered oxide etch. The GaAs segment was successfully grown from the Au catalyst sitting on top of each Si nanowire. We observed that, during the temperature rise up to the GaAs growth temperature, Au diffuses on the side walls of the Si nanowires and induces the growth of lateral GaAs needles. Additional defects were observed such as GaAs shells and segment kink at the GaAs/Si interface (see Fig. 1). Surface treatments and growth parameters will be discussed.

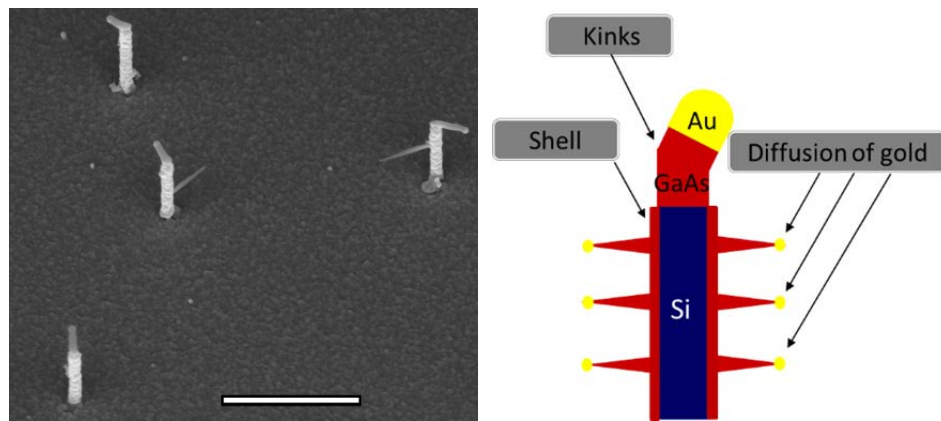


Figure 1. SEM image of GaAs/Si nanowires (scale bar 1  $\mu\text{m}$ ) and schematic representation of the main challenges related to GaAs/Si nanowire growth.

## References:

<sup>1</sup> F. Glas, *et al.*, *Physical Review B* 121302(R), (2006)

<sup>2</sup> H. Kroemer, *et al.*, *Journal of Crystal Growth*, **81**, 193–204 (1987);

<sup>3</sup> I. J. Luxmoore, *et al.*, *Scientific reports* **3** (2013);