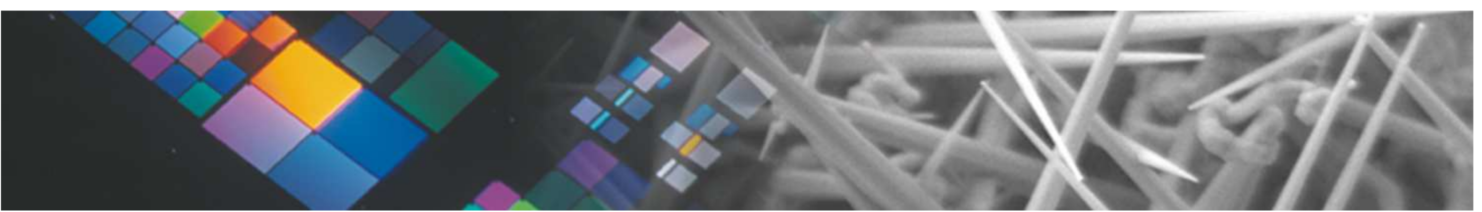

Heterogeneous integration and applications in electronics

leti

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What kind of functionnalities can be addresses by nanomaterials and nanostructures grown on a substrate ?

How to integrate nanomaterials in devices with an added value ?

OUTLINE

- Nanocrystals for memory devices
- Nanowires for low power devices, capacitors and sensors
- Thin films : SiGe (D. Dutartre) and III-V (B. Kunert) on a Si platform for NMOS and PMOS FET

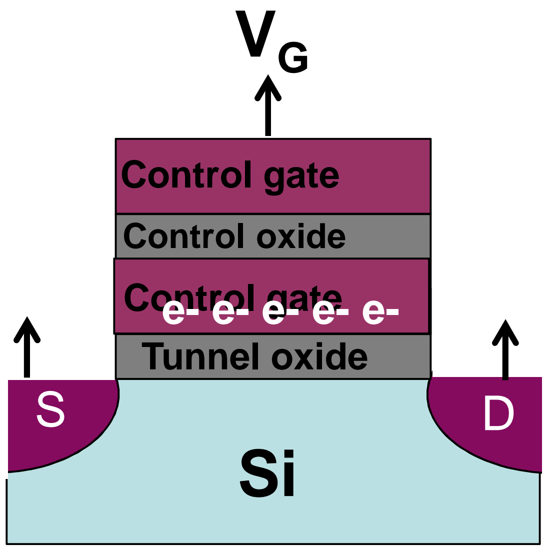
OUTLINE

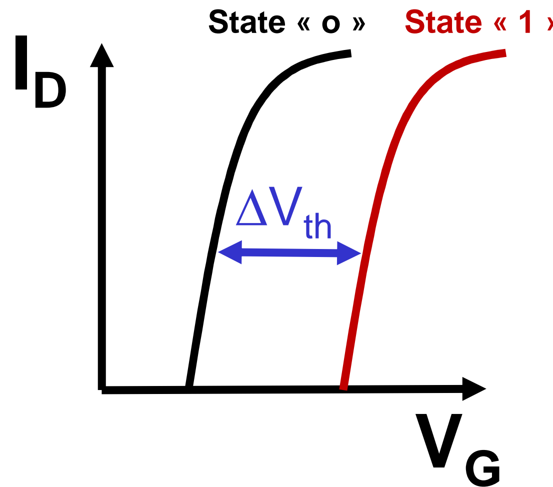
- Nanocrystals for memory devices
  - Principle
  - Nanocrystal growth
  - Integration in devices

- Nanowires for low power devices, capacitors and sensors

- SiGe and InGaAs thin films for NMOS and PMOS FET

- Flash memory = MOSFET + floating gate
- Electron storage in floating gate ➔ shift Id-Vg characteristic



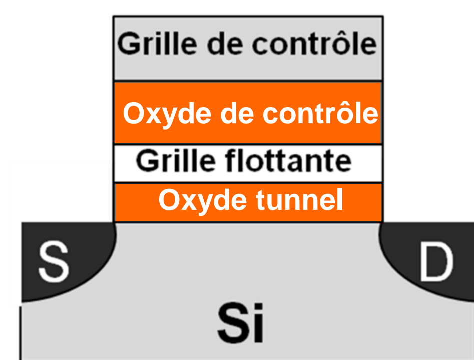


- Two different states due to the presence of charges in the floating gate

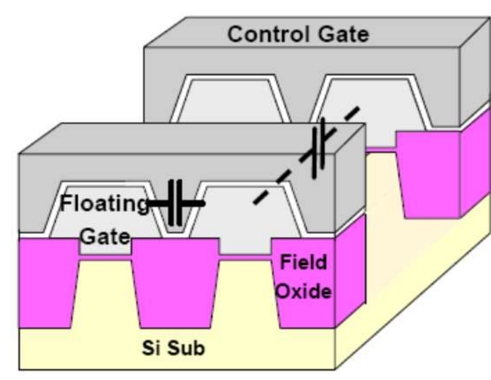
Flash memories principles

Standard Flash memories :

- Limitation of reducing the thicknesses of dielectric [1] :
  - ✓ tunnel oxide t > 6nm (SILC)
  - ✓ Control oxide EOT > 10nm



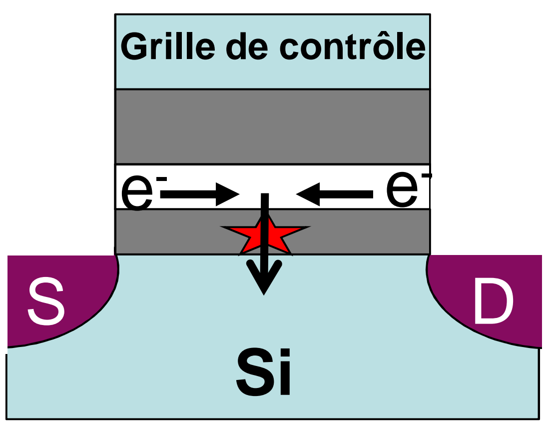
- Spacing reduction between memory cells :
  - ✓ Parasitic coupling between floating gate [2]
  - ✓ Decrease of the capacitive coupling between the floating gate and the channel (lateral extension of the gate)

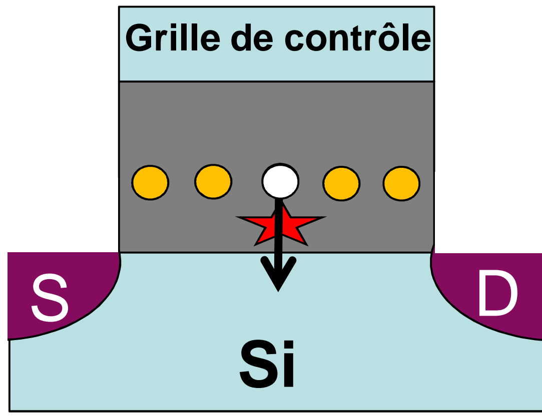


[1] S. Lai et al., Int. non volatile memory conf. 1998 [2] K. Kim, IEEE Proc. Of IEDM 2005

Interest of nanocrystals memories

- Decrease of the tunnel oxide without compromise with charge retention :





- Decrease of the parasitic capacitive coupling between cells [1]
- Multilevels storage
- Decrease of the fabrication cost by decreasing the number of lithographic masks needed
- **NC advantages : more robust devices against defects**

[1] G. Molas et al., Proc. Of IEDM 2007

OUTLINE

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Choice of CVD for nanocrystal growth

- Uniform distribution over large areas
- Uniform thickness and composition over large areas
- Selective area deposition because of different activation energies for reaction with different surfaces
- Objectives : high nc density and low size dispersion
  - For high charge storage and low device variability

CVD

Thermal CVD	Plasma CVD	Photo CVD	Catalytic CVD	CVI
APCVD	PECVD		Hot-wire	
LPCVD	DC CVD		CNT	
HTCVD	RF CVD			
MTCVD	MW CVD			

Reaction gas premixing

Membrane valves

Filter 2 µm

Mass Flow Controller

Check valves

H_2

Ar

100-5000 sccm

MFC 1

SiH_4

100%, or 10%, 1% in H2

10-500 sccm

MFC 2

H_2

O_2

Cl_2

10-500 sccm

MFC 3

CH_4

C_3H_8

H_2

100-5000 sccm

MFC 4

P_{in}: 3 bar

$SiCl_4$

Bubbler

bypass

Inductive reaction furnace (1300 °C)

20-100 kHz

Quarztube

Coil

Pirani

0,1 – 1000 mbar

Pressure controller

Cyclon

cooling trap

Exhaust gas

Vacuum pump

$65 m^3/h$

Exhaust cleaning

Si deposition by CVD on amorphous substrates

- Silane dissociation reactions :

$$SiH_4(g) \rightarrow SiH_4\ (ad)$$
$$SiH_4\ (ad) \rightarrow SiH_2\ (ad) + H_2\ (ad)$$
$$SiH_2\ (ad) \rightarrow Si + H_2\ (ad)$$
$$H_2\ (ad) \rightarrow H_2\ (g)$$

- $V_{dépôt} = C\ P^a \exp(-E_a/kT)$
- Si nanocrystals nucleation study on amorphous substrate:

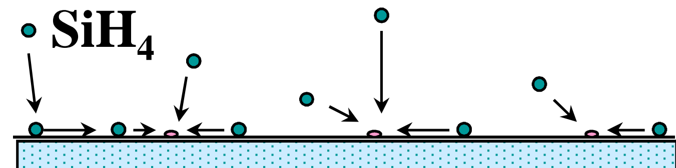
➢ Experimental parameters (T, P_{SiH4})

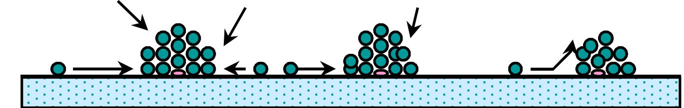
➢ Chemical nature of the substrate (SiO_2, Si_3N_4, Al_2O_3)

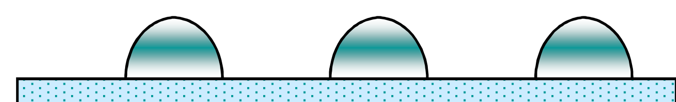
Si deposition by CVD on SiO_2

Volmer Weber 3D growth mode

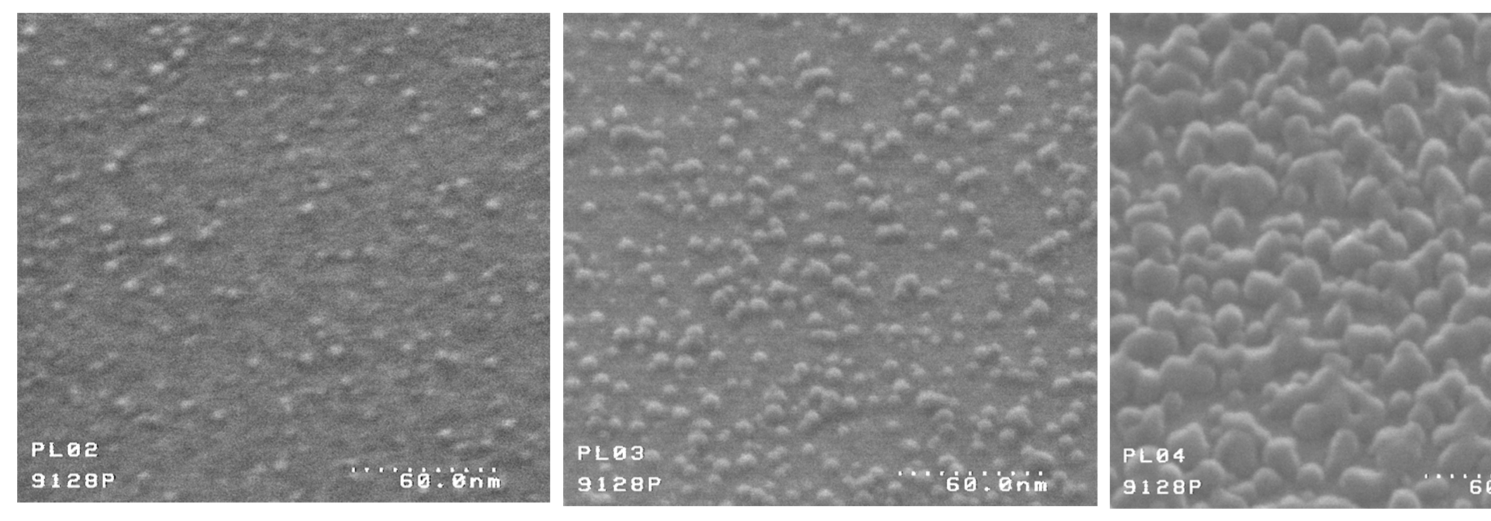
500
250
0
0 250 500 нм

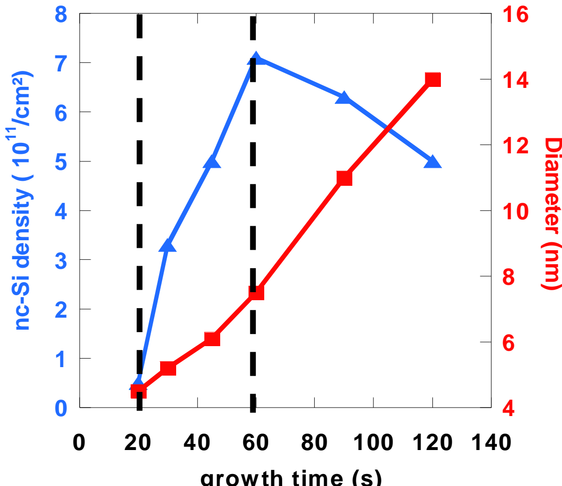






Growth time influence



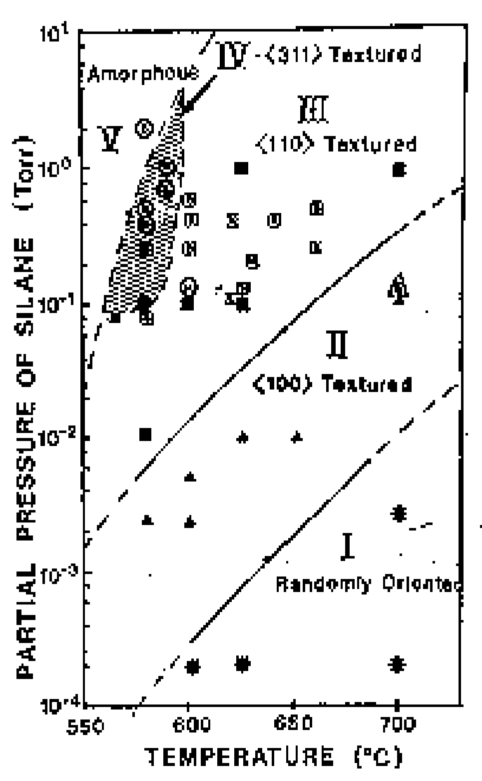


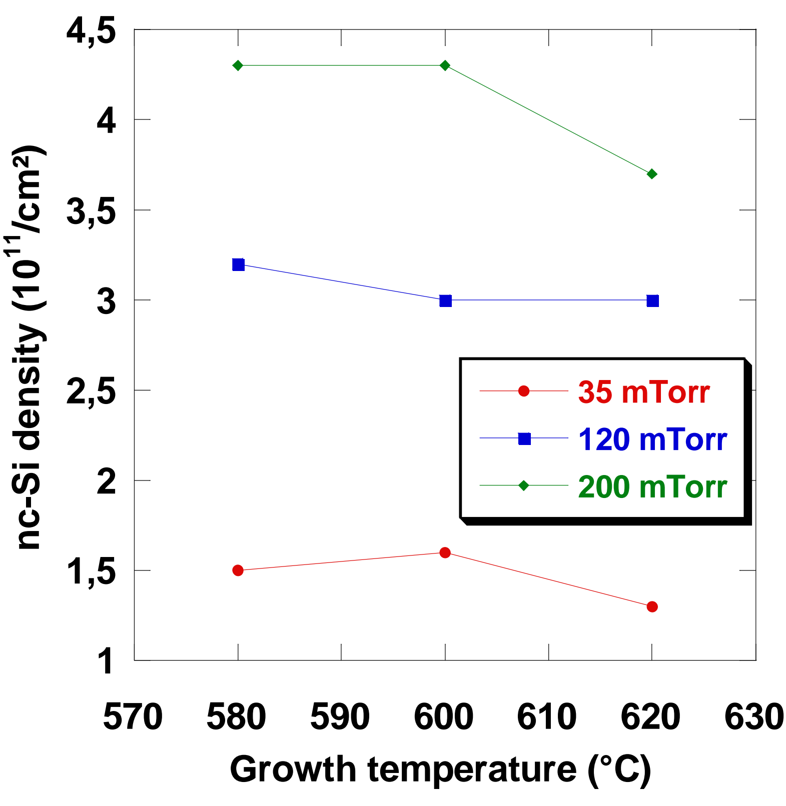
P_{SiH4} and growth temperature constants

1. Nucleation
2. Growth
3. Coalescence
4. Formation of continuous Si film

F. Mazen, PhD Thesis 2003

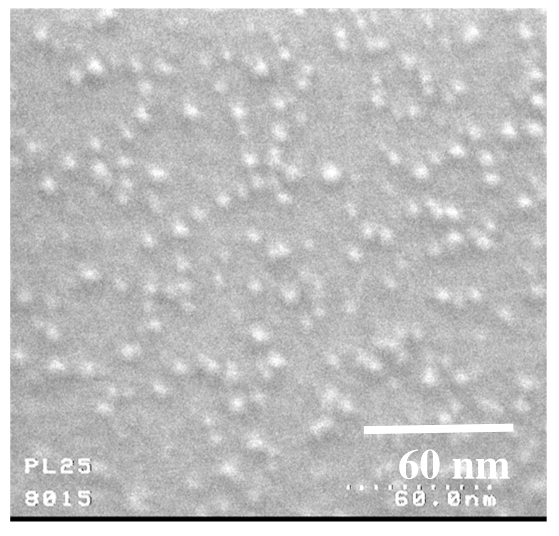
Influence of P_{SiH4} and $T_{substrate}$





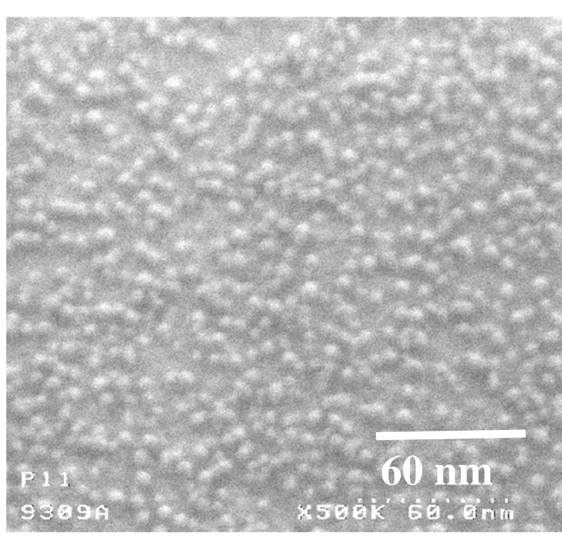
- Low effect of temperature on Si nucleation (range 570-620°C)
- P_{SiH4} promotes Si nucleation

Influence of substrate surface chemistry



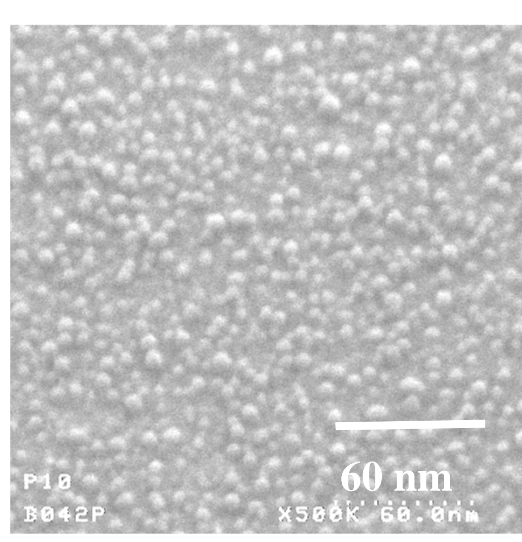
SiO_2

$3x10^{11}$ Si-Ncs/cm^2



Si_3N_4

$9.5x10^{11}$ Si-Ncs/cm^2

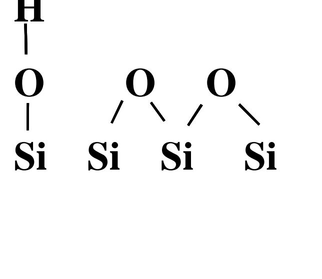


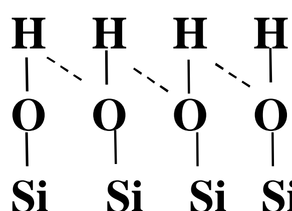
Al_2O_3 (ALD)

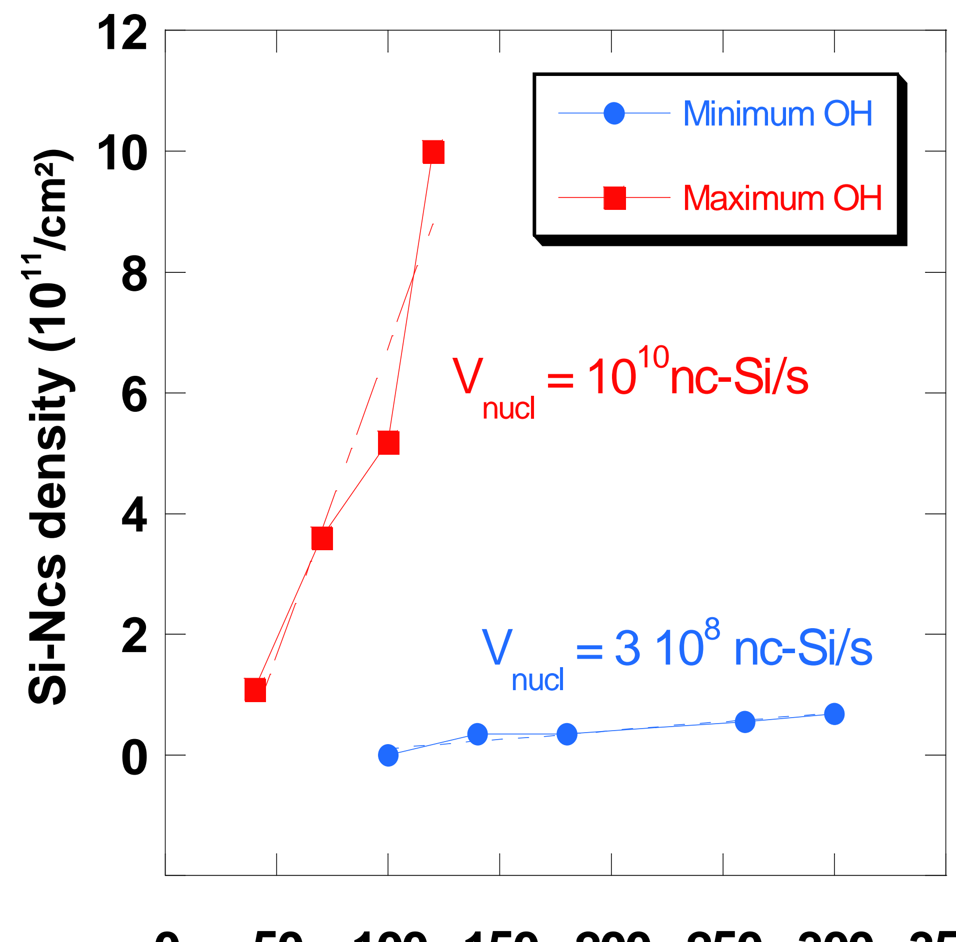
10^{12} Si-Ncs/cm^2

- ❑ Thermal SiO_2 is not favourable for a high Si-Ncs density (strong Si-O bonds)
- ❑ On deposited Si_3N_4, strong nucleation (rugosity, defects…)
- ❑ On Al_2O_3 deposited by Atomic Layer Deposition, OH groups favour Si nucleation

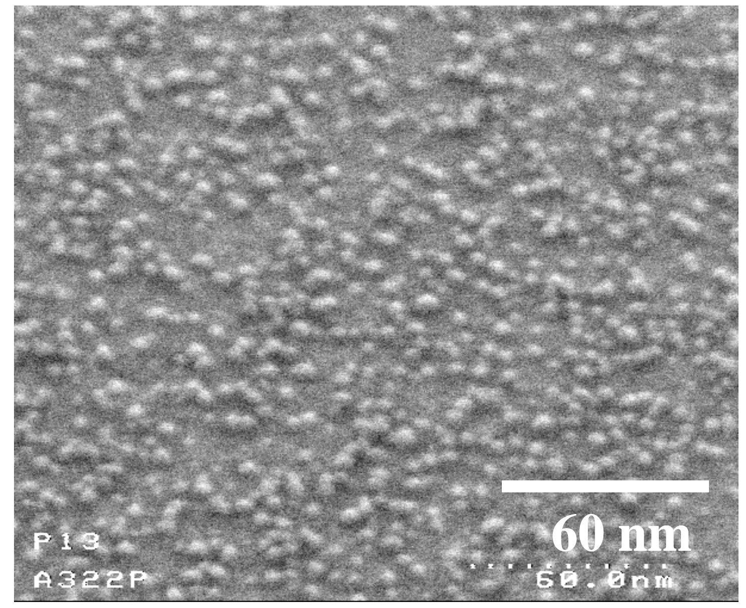
Influence of OH groups on SiO_2 substrate

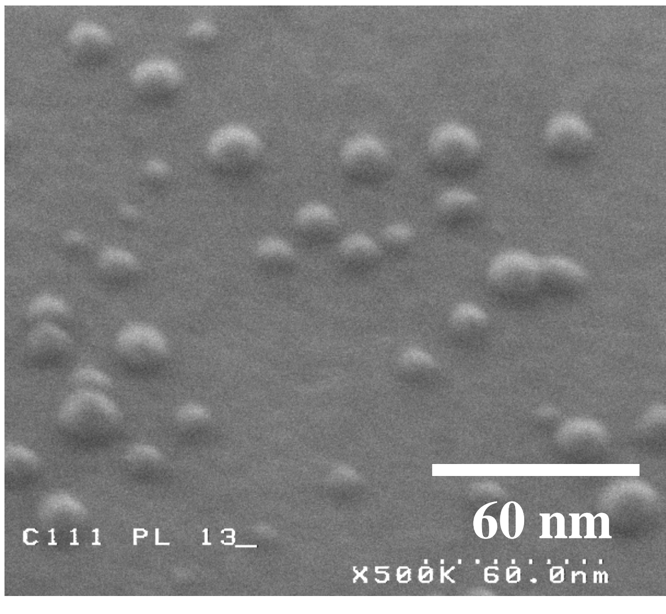






Influence of OH groups on SiO_2 substrate





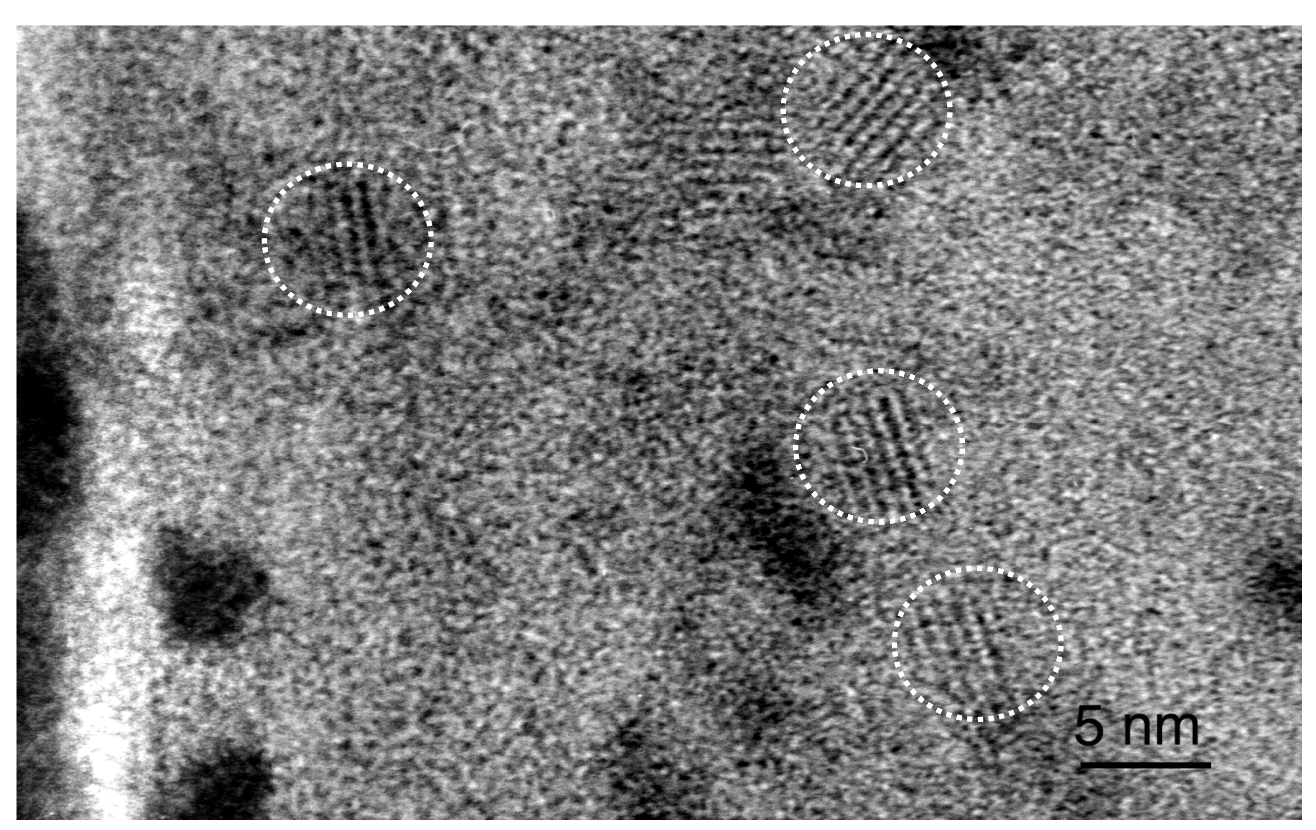
HF treatment
Density : 10^{12} Si-Ncs/cm²

As grown SiO_2
Density : 7 10^{10} Si-Ncs/cm²

- Si-OH groups govern the Si nucleation on SiO_2

JECS 150, G203 (2003)

Structural characterization by TEM



- ❑ **nc-Si are crystalline**

Size dispersion

Large size dispersion for nanocrystals = 30%

Densité de nc-Si (10^{11}/cm²)

4
3,5
3
2,5
2
1,5
1
0,5
0

Nucleation period

50 100 150 200 250

Temps de dépot (s)

Nucleation occurs during all along the growth

SiH_4

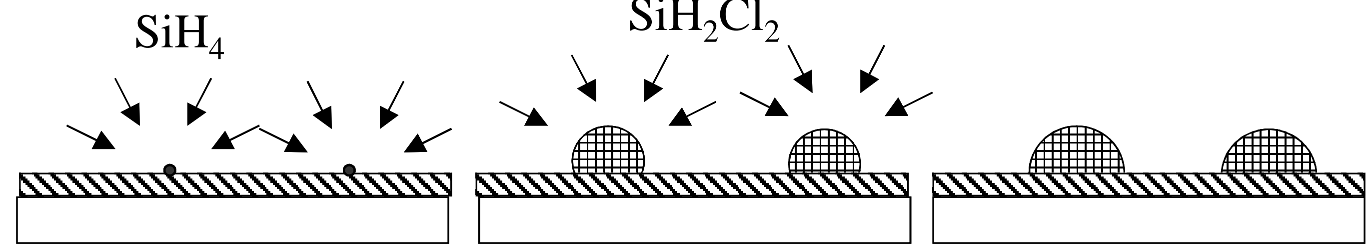
4

SiH_4

substrat

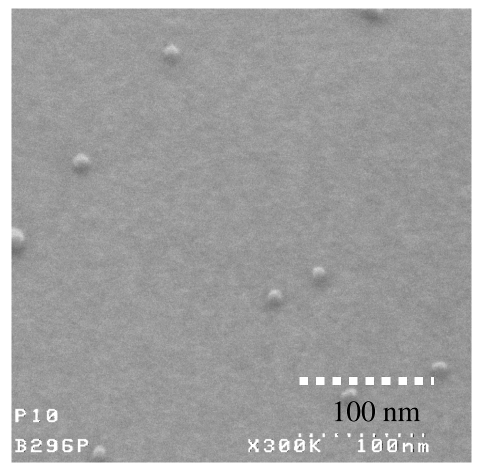
diélectrique

Solution : separate nucleation and growth steps



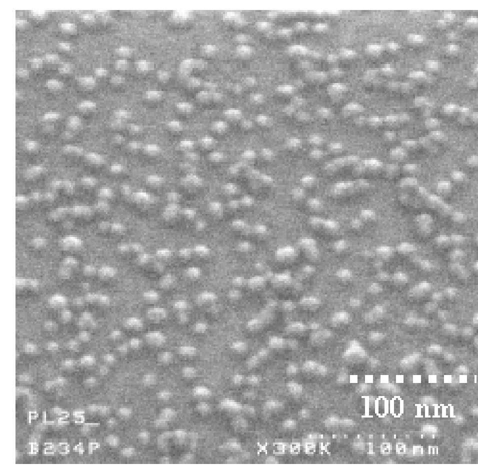
Step 1 influence

60 mTorr SiH_4



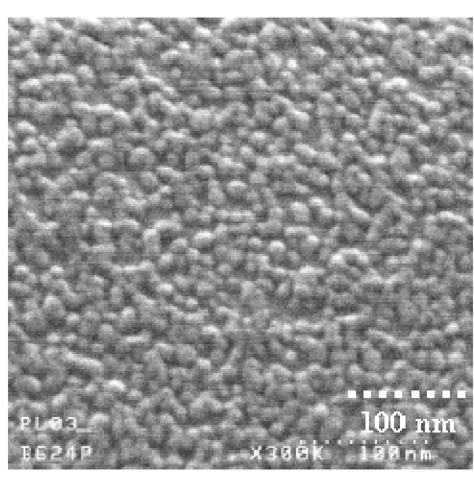
5×10^9 nc-Si/cm²

200 mTorr SiH_4



3×10^{11}nc-Si/cm²

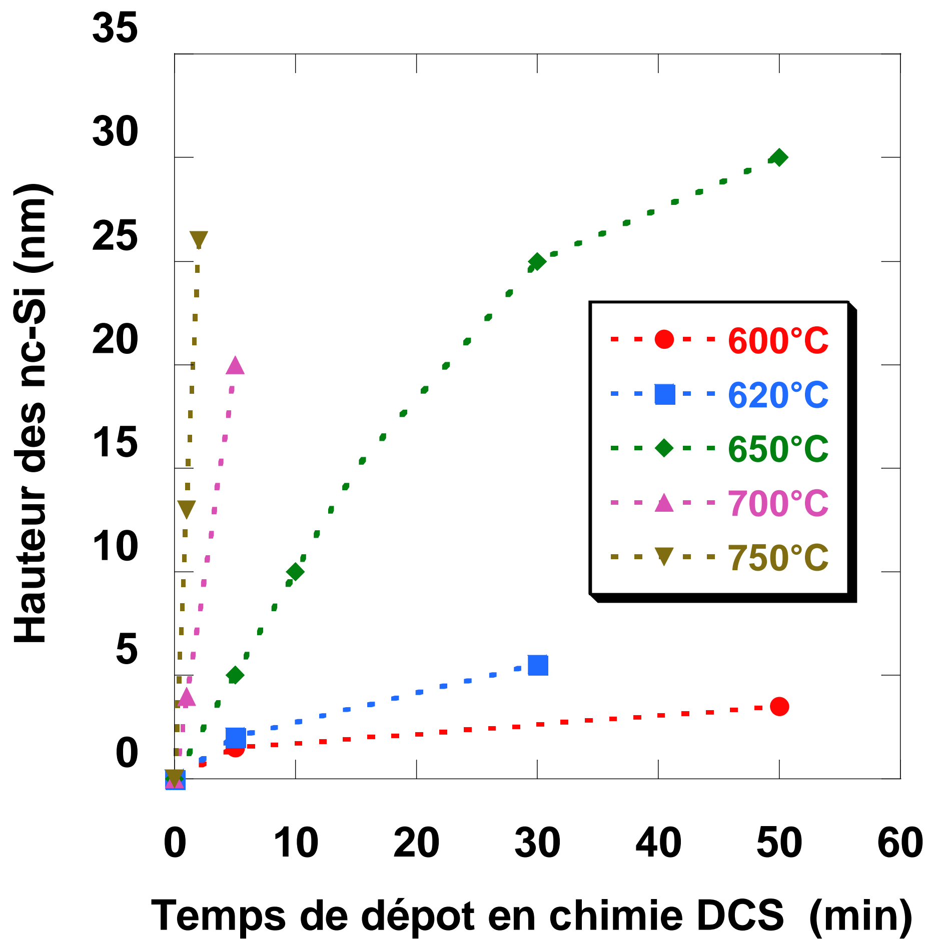
200 mTorr SiH_4
With HF treatment



7×10^{11}nc-Si/cm²

Step 1, exposition of the surface to SiH_4 for a short time, control the nanocrystal density

Step 2 influence

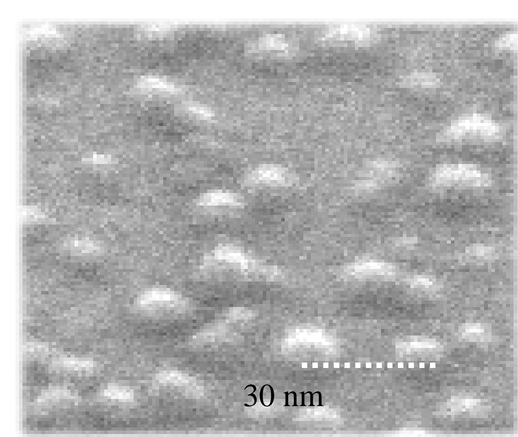


Step 2, exposition of the Si nuclei to SiH_2Cl_2 control the growth rate and hence the size of the nc (0.001 à 13 nm/minute)

Size dispersion

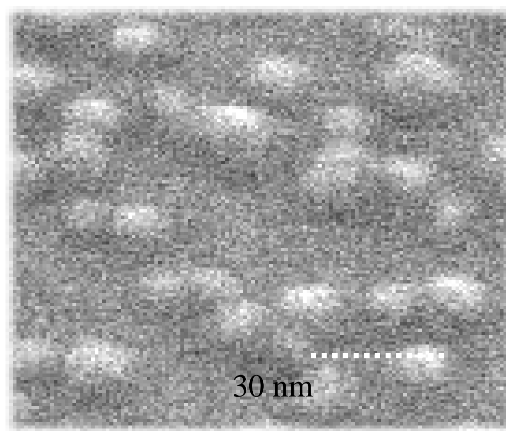
1 step SiH_4

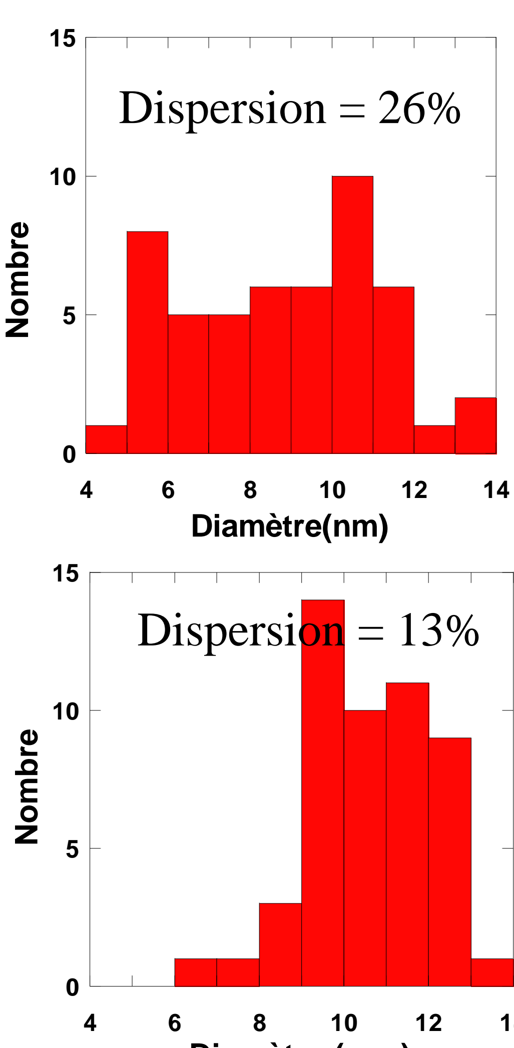
Density: 2.8 10^{11}/cm²
Diameter : 9 nm



2 steps $SiH_4 + SiH_2Cl_2$

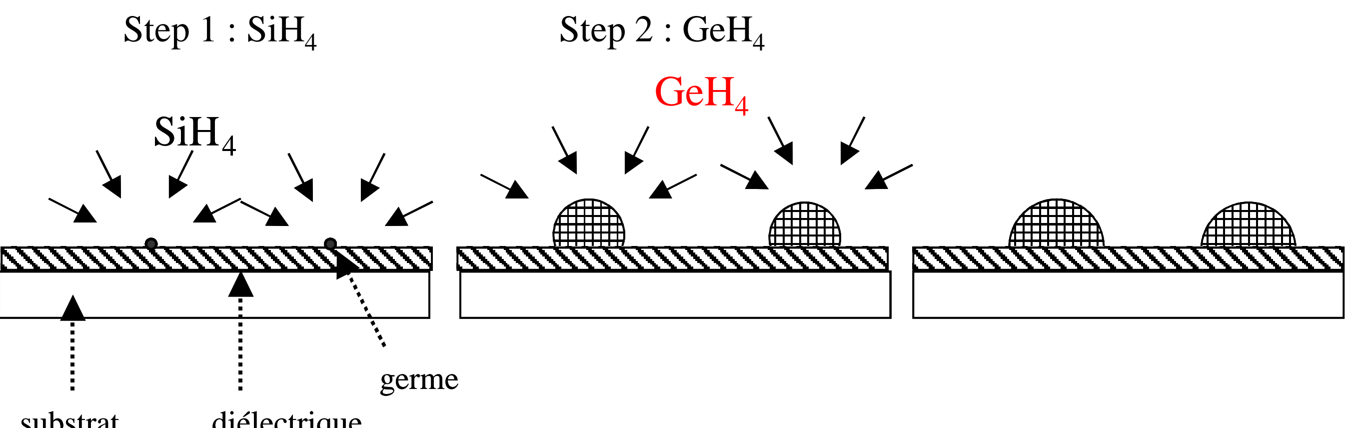
Density: 3.1 10^{11}/cm²
Diameter : 11 nm

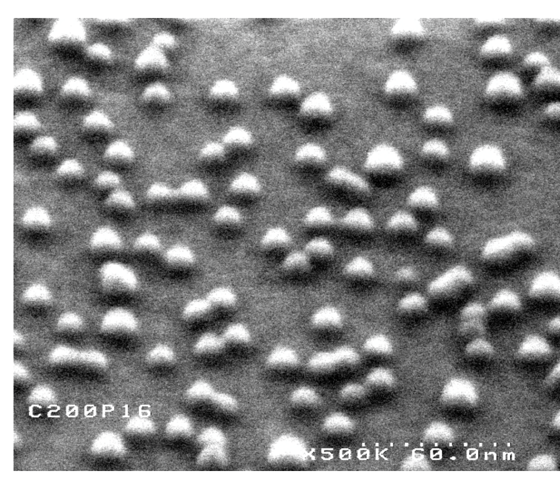


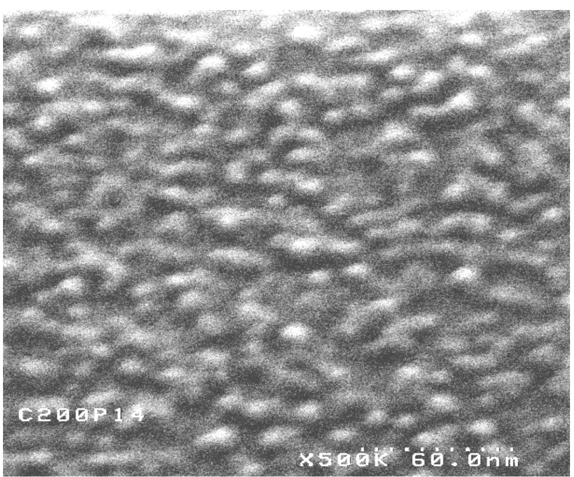


Possibility to elaborate Ge nanocrystals

GeH_4 : almost no Ge nucleation on SiO_2





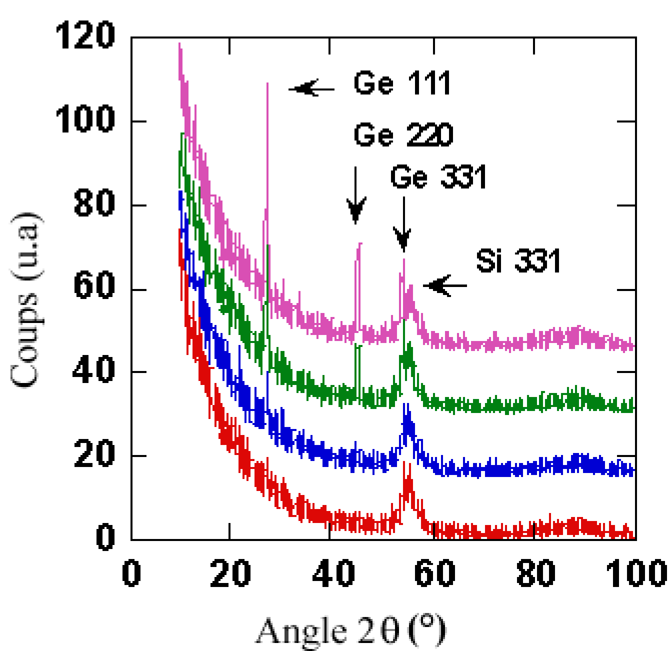


Density : $2x10^{11}$
Diameter : 12 nm

Density : $6x10^{11}$
Diameter : 7 nm

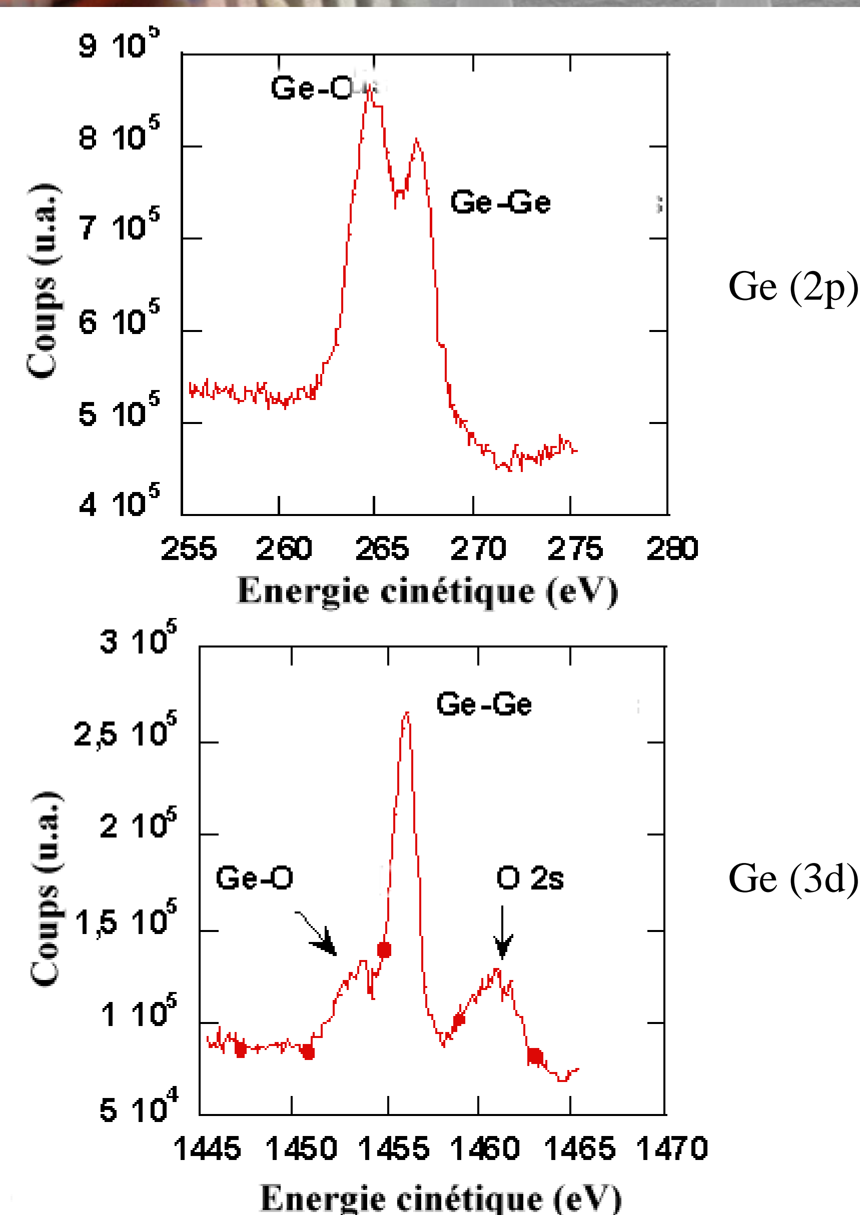
Structural characterization of nc-Ge

XRD



Nc-Ge cristallins with GeO_x shell

XPS

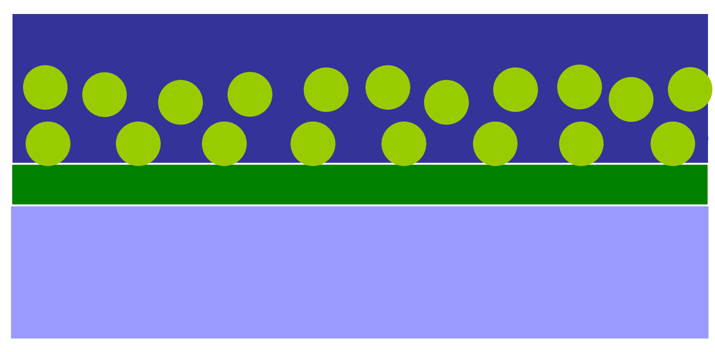


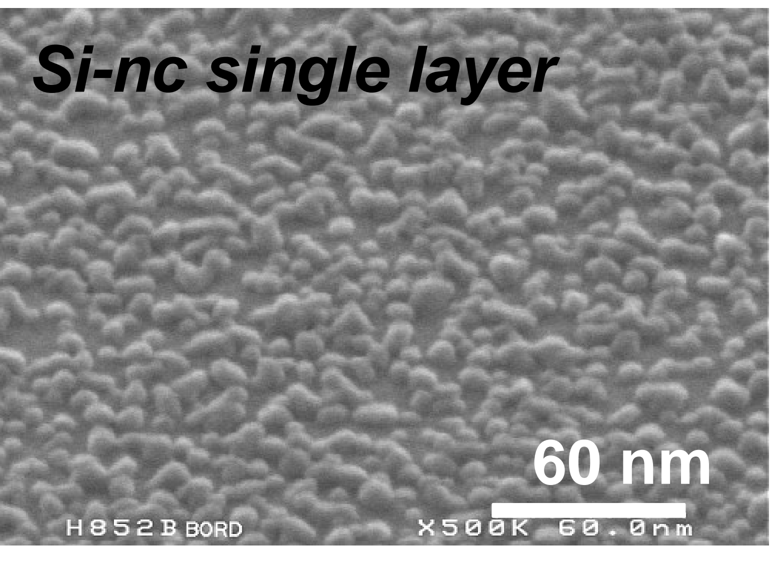
Ge (2p)

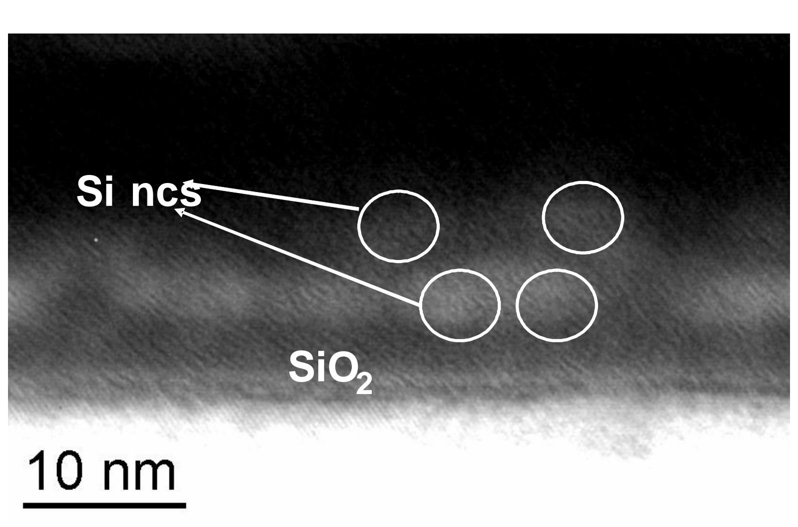
Ge (3d)

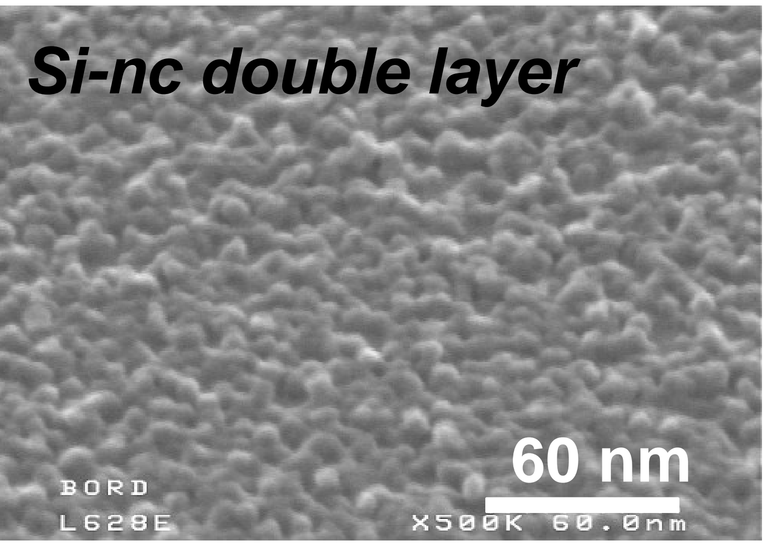
Si-nc double layers – Basics

Objective: deposition of 2 layers of Si-ncs to improve the nc-Si density









OUTLINE

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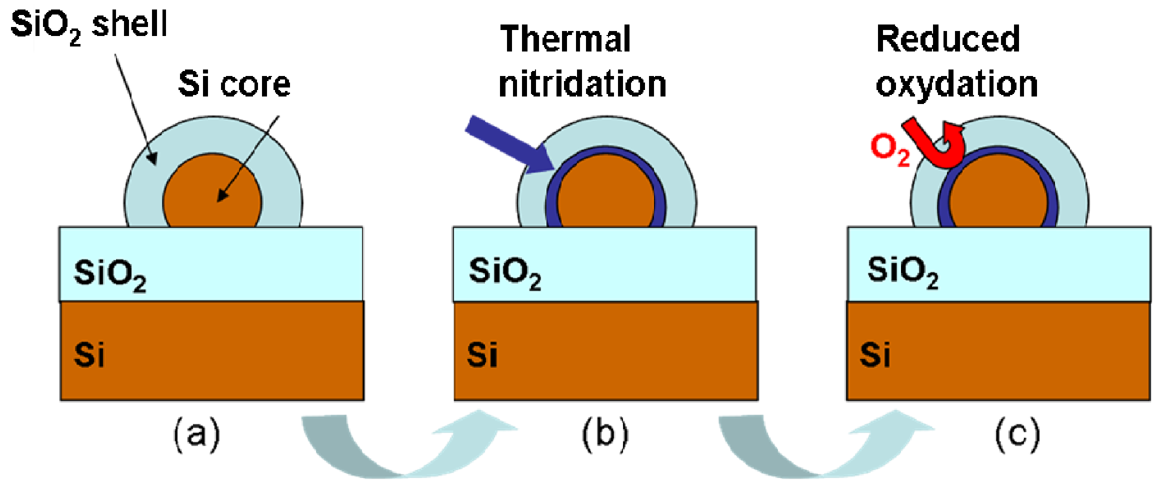
Passivation of Si-nc by nitridation

- Nitridation effects
  - Si_3N_4 O_2 diffusion[1] is imited
  - NO et NH_3



[1] M.L. Green *et al.*, APL 67(11), p 1600, (1995)

[2] K. C. Scheer *et al.*, APL 93 (9), p 5637, (2003)

Thèse J. Dufourcq
P. Mur, O. Renault, CEA-Leti
S. Bodnar, ATMEL,

Selective deposition of SiN on Si-nc

Ramp up
DCS

T Stab +
nucleation SiH_4

T Ramp up
N_2

Nitride dep
$DCS+NH_3$

T Ramp down
N_2

1

2

3

J. P. Colonna et al., MRS

16e V

25e V

50 nm

(d)

60nm

3nm

HTO

SiN

Si

Si-ncs capped with SiN shell : hybrid Si-nc SiN trapping layer

G. Molas et al., IEDM 2007

XPS simple description

e⁻ top layer
e⁻ lower layer with collisions
e⁻ lower layer but no collisions
X-Rays
Outer surface
Inner surface
Atoms layers

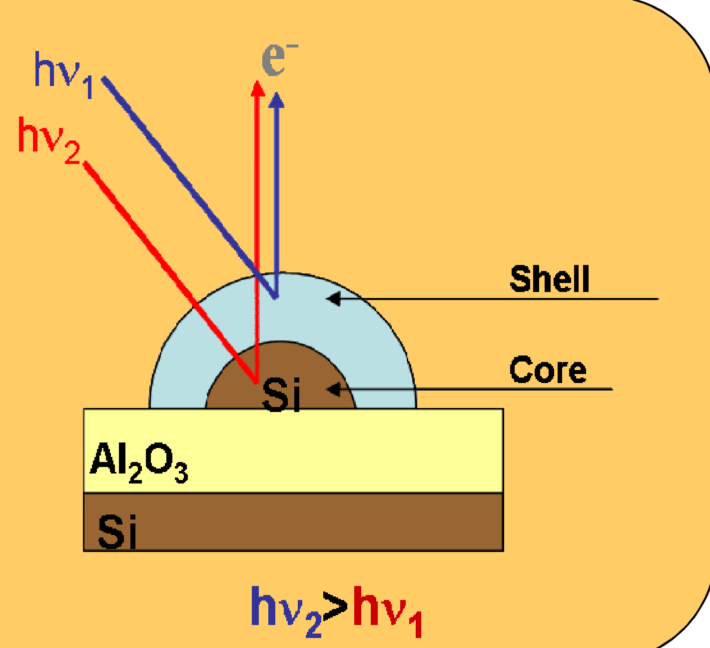
XPS analysis of nitrided NC-Si

XPS VUV ELETTRA Synchrotron :

- Energy resolution (0.05 eV/0.5 eV for laboratory equipment)
- Energy screening (depth profil)

- <u>Analysis condition :</u>

➢ Shell :		Si(2p) e- hν=160eV
		N(1s) e- hν=400eV
➢ Core + shell :		Si(2p) e- hν=250eV
		N(1s) e- hν=700eV

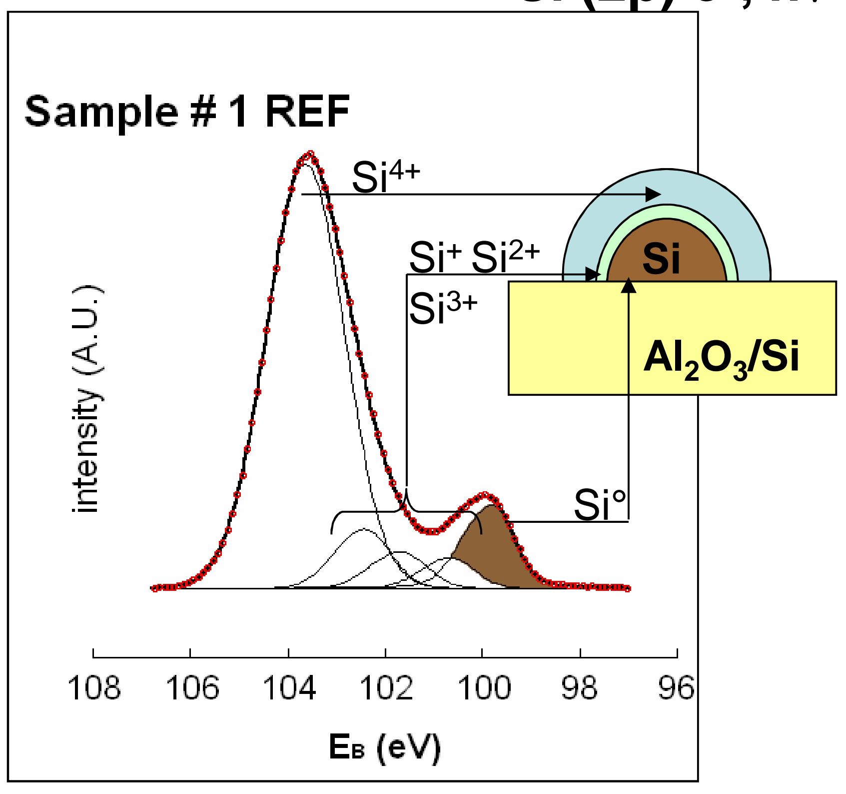


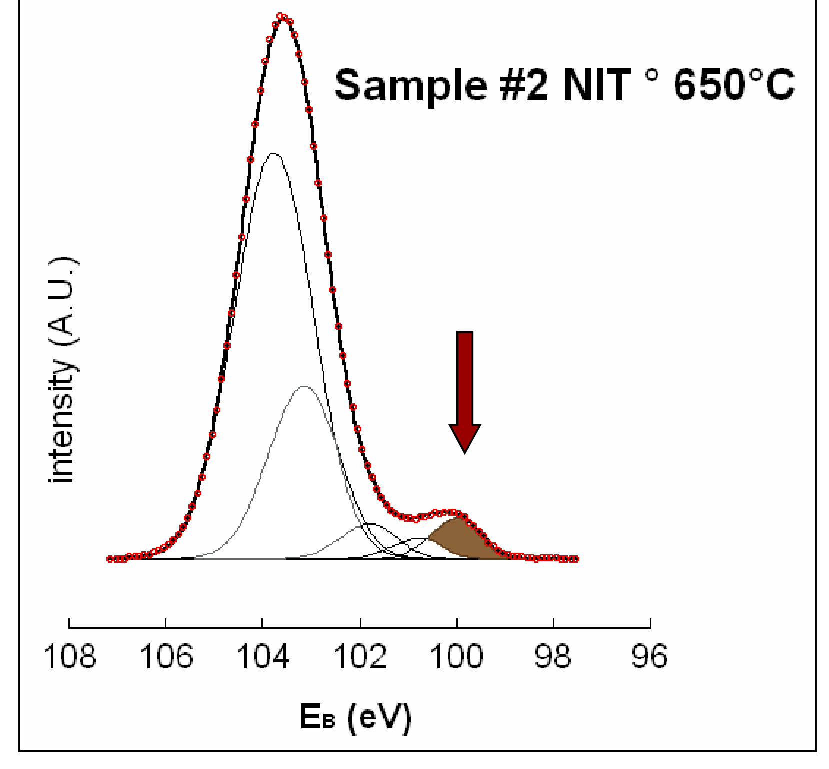
- **Samples :** **Density : 8E11 cm^{-2}** **∅ = 8nm**

#1 = REF	#2 = NIT° 650°C	#3 = NIT° 750°C
Si dots (CVD)	REF	REF
+	+	+
Chemical SiO2 (O_3)	Nitridation NH_3 650°C	Nitridation NH_3 750°C

XPS analysis of nitrided NCs-Si

Si (2p) e-, hν = 160 eV





REF * :
Si° : core
Si^{+} Si^{2+} Si^{3+} : Interface core/shell
Si^{4+} : shell SiO_2

Nitrided sample at 650°C :
⇒Shell growth
⇒ presence of Si core

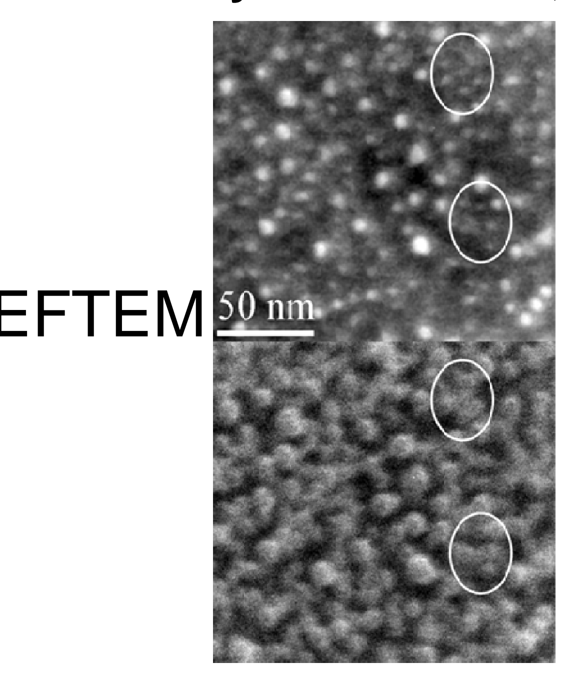
* O. Renault et al., APL **87**, 163119 (2005)

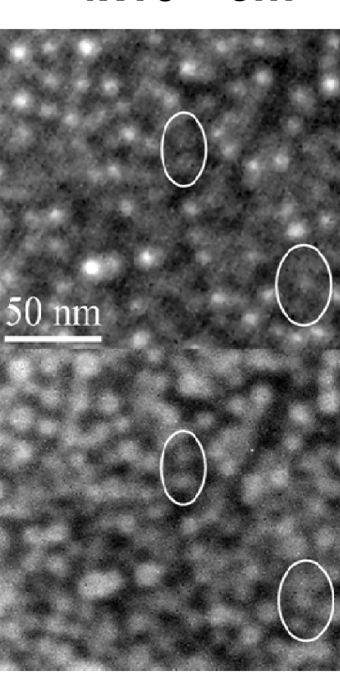
TEM analysis of nitrided Si-nc

Density : 8×10^{11} cm^{-2}, 4×10^{11} cm^{-2}

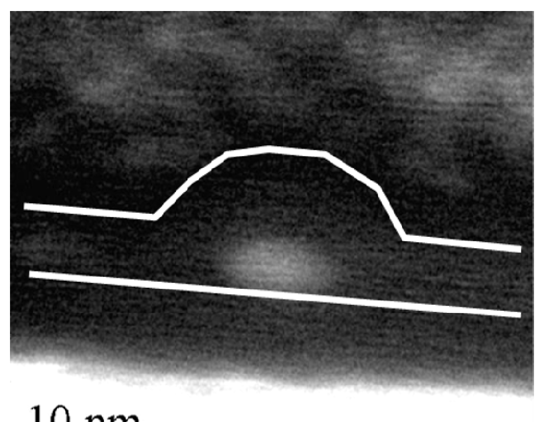
S. Lombardo et al., IMM

EFTEM





Reference, nitridation at 750°C



Cross section TEM

SIMS profile

Nanocristaux/SiO$_2$ (5nm) + nitruration NO

Nanocristaux/SiO$_2$ (5nm) + nitruration NH$_3$

[SiO$_2$ (5nm) + nitruration NO] + Nanocristaux non nitrurés

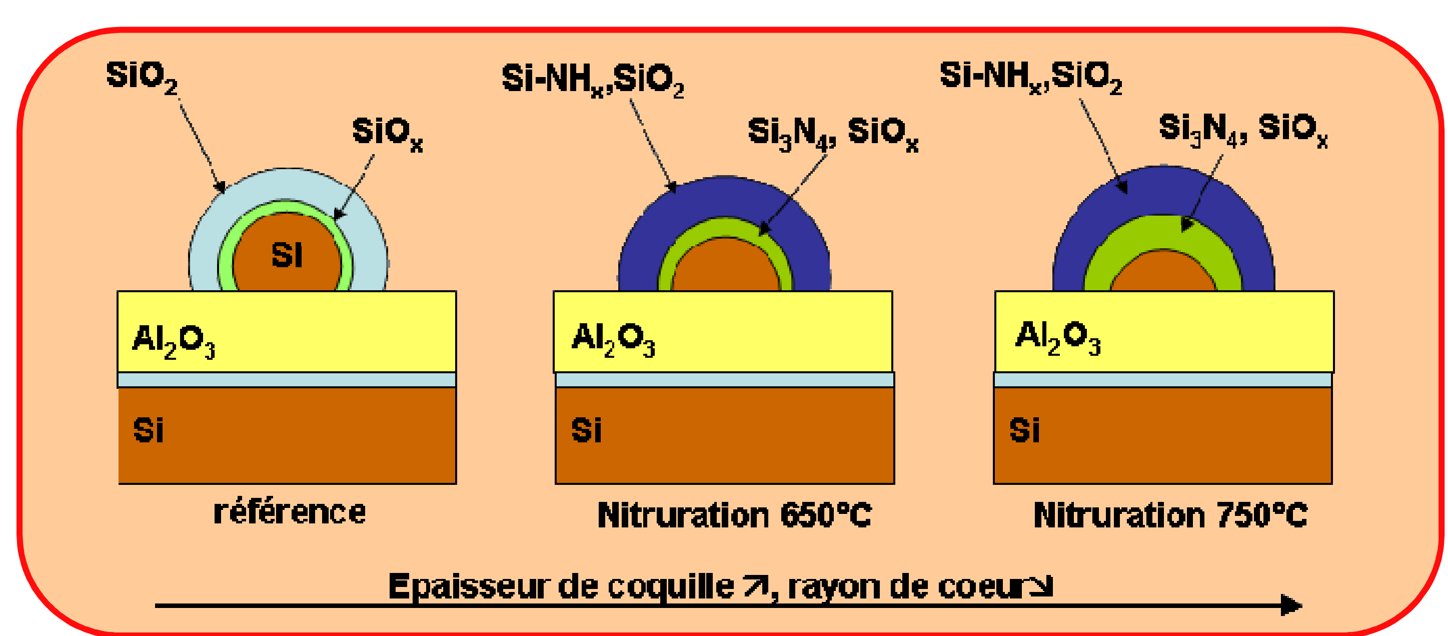
[at/cm3] [cnt/s] [nm]

Conclusion :

- Si nanocrystals density reduction
- N located preferentially at the surface

J. Dufourcq, PhD thesis 2008

NC-Si nitridation



32Mbits memory devices 130 nm node

	Echantillon 1	Echantillon 2	Echantillon 3	Echantillon 4
MEB	60 nm	60 nm	60 nm	60 nm
TEM vue plane	50 nm — 4 nm	50 nm — 6,5 nm	50 nm — 8 nm	50 nm — 12 nm

Erased — 512Kb — Number of bits vs Threshold Voltage (V) — Sample 1, Sample 2, Sample 3, Sample 4

Written — 512Kb — Number of bits vs Threshold Voltage (V) — Sample 1, Sample 2, Sample 3, Sample 4

*Thèse de doctorat Stéphanie Jacob, 2008

Industrial ncs-Si memories

Freescale

Split gate structure

(a)
Kinetis Microcontroller
TFS FLASH

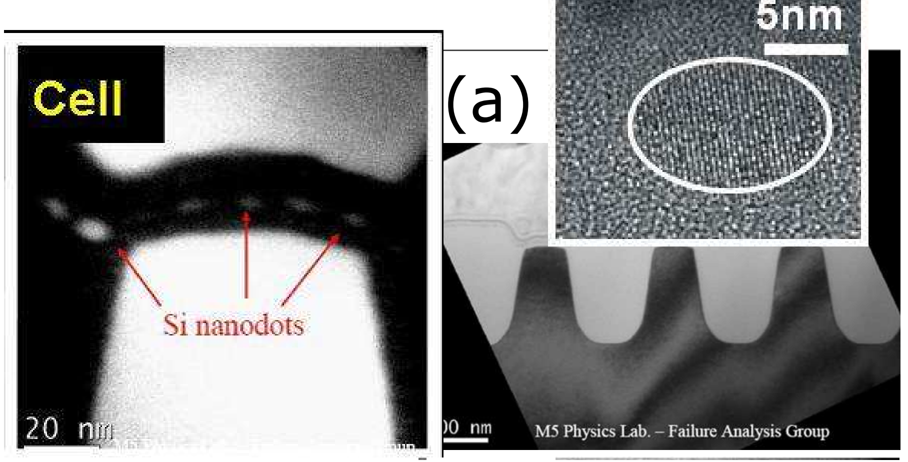
Number of Bits
50K Cycles
100K Cycles
300K Cycles
~2V operation window at 300K cycles
Cell Vt [V]

Kang et al.,VLSI 2008, IMW 2009, IMW 2012

Commercial products:
Embedded memories for microcontrolers in 90nm technology

STMicroelectronics

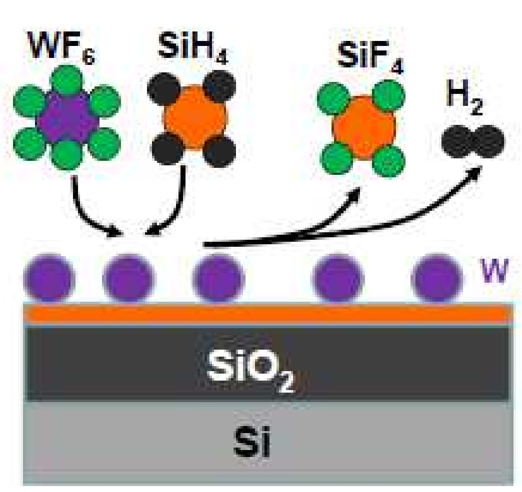
Architecture NOR 4Mb

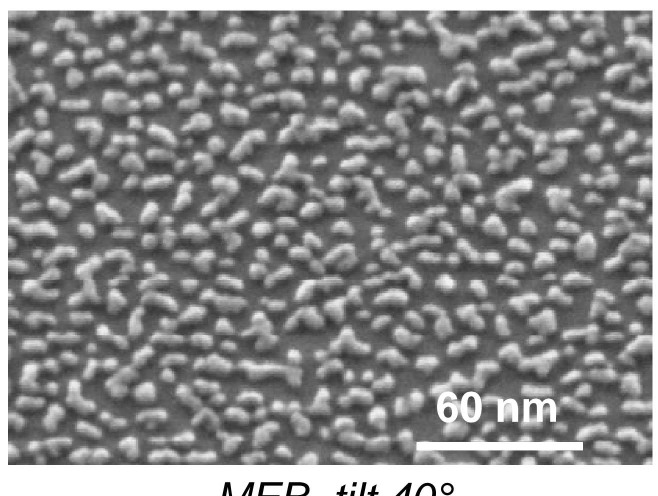


Gerardi et al., IEDM2008

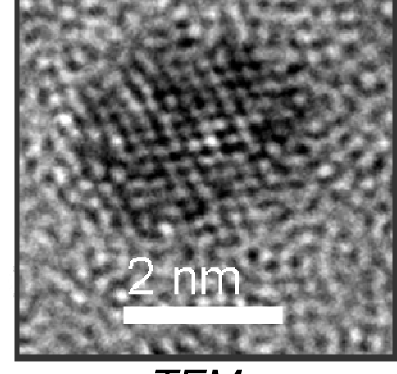
metallic NC deposited by CVD

- W advantages :
  - ✓ refractory material (T_{fusion} = 3410°C)
  - ✓ Stable with SiO_2
- Precursors : $WF_{6\,(g)}$ et $SiH_{4\,(g)}$





MEB, tilt 40°



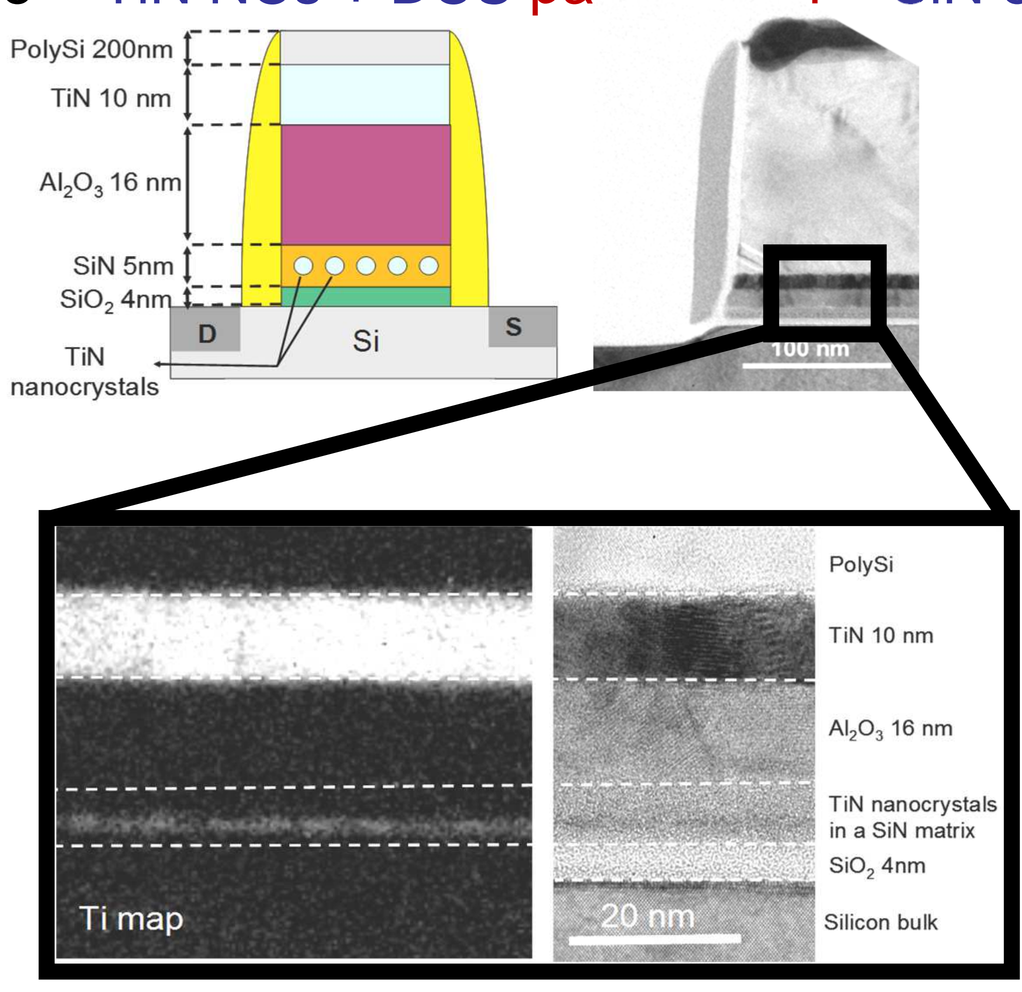
TEM

Density : 7.10^{11} cm^{-2}
Diameter moyen : 6 nm

TiN NCs

Memory devices integrating metallic nanocrystals:

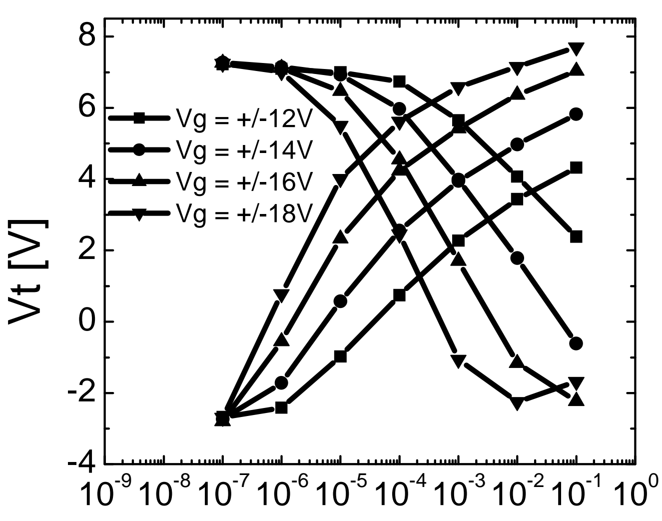
Floating gate = TiN NCs + DCS passivation + SiN encapsulation

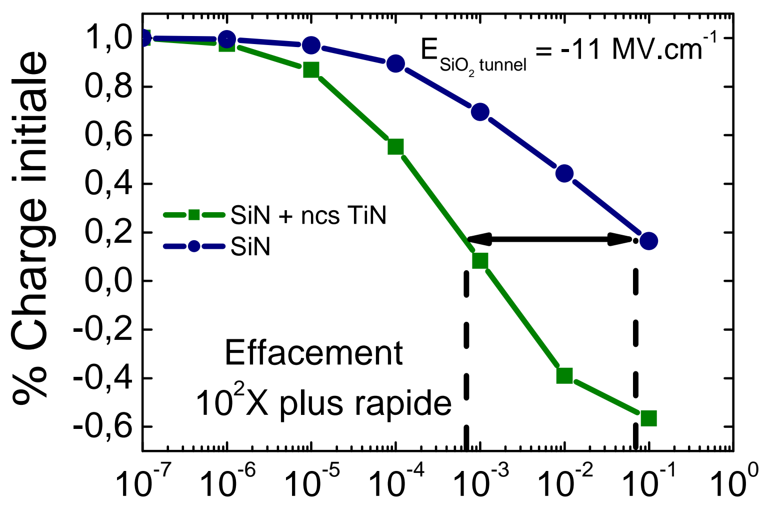


G. Gay, PhD, 2011

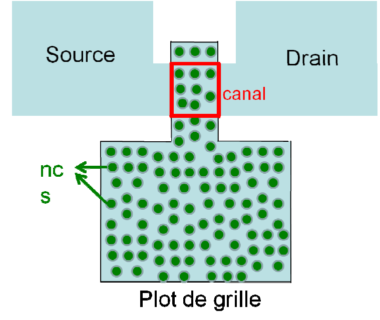
Performances of TiN NCs memories

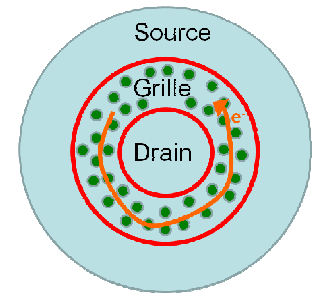
- Functional devices
- Gain in writing speed, and memory windows





- Retention could be optimized by decreasing the nanocrystals density (lateral leakage of charges)





Conclusions

- CVD allows to grow directly Si, Ge and metallic nanodots
- Control of density and size dispersion possible if nucleation and growth decoupled
- Selective growth possible
- Core / shell nanostructured and passivation possible

- Large scale integration of nanolayers and nanostructures unable by CVD

- Semiconductors, metals, oxydes nanodots ….

VLS growth and applications of $Si/Si_{1-x}Ge_x$ nanowires

OUTLINE

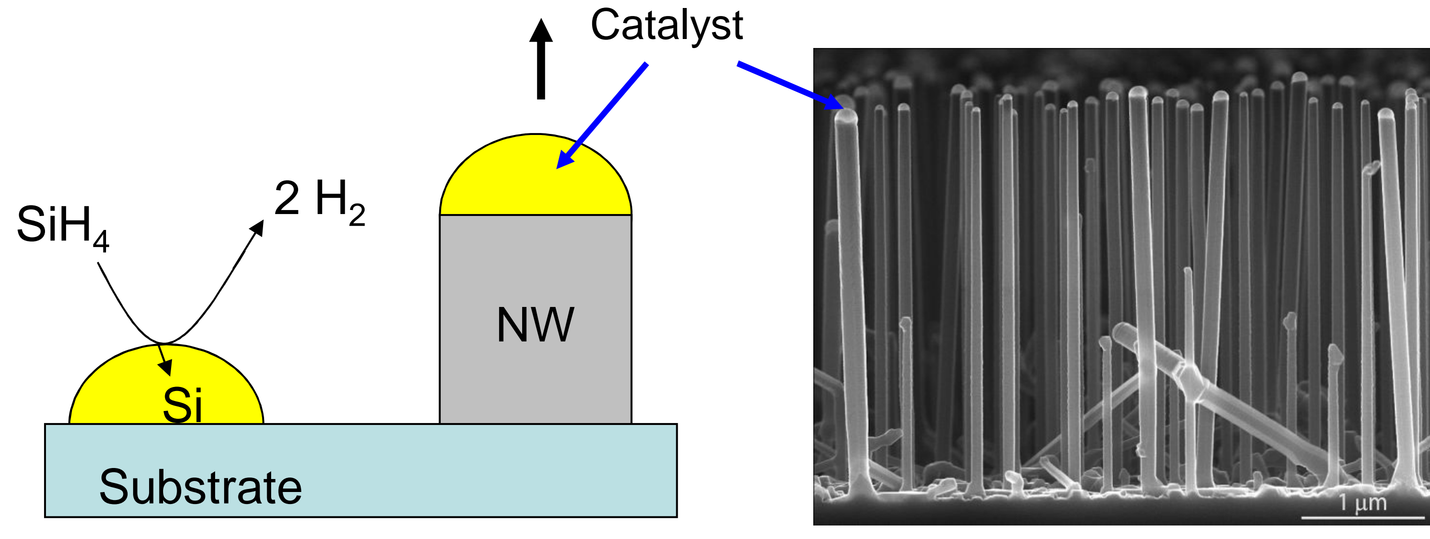
- Nanocrystals for memory devices

- Nanowires for low power devices, capacitors and sensors
  - Objective
  - Si/SiGe nanowires catalytic growth
  - Other applications

- SiGe and InGaAs thin films for NMOS and PMOS FET

Introduction : CVD – VLS nanowires growth

Ellis et Wagner, 1964

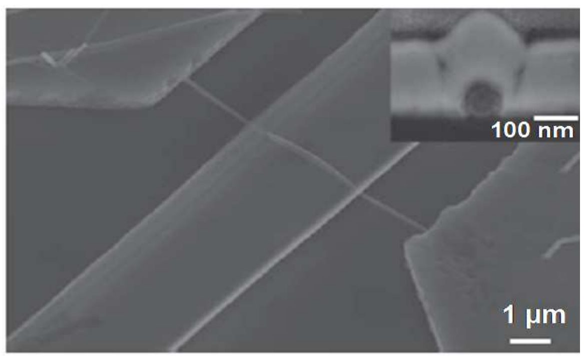


[Oehler10]

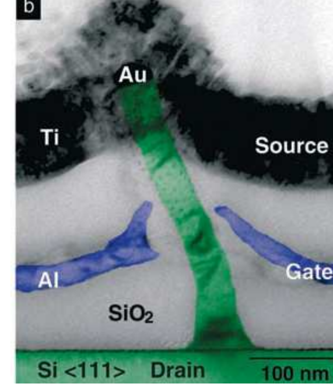
- Crystalline growth possible without any epitaxy relation
- Nanometric diameter without lithographic steps
- Low temperature synthesis < 450°C compatible with back-end process
- High aspect ratio
- High surface/Volume ratio

Nanowires applications

Transistors

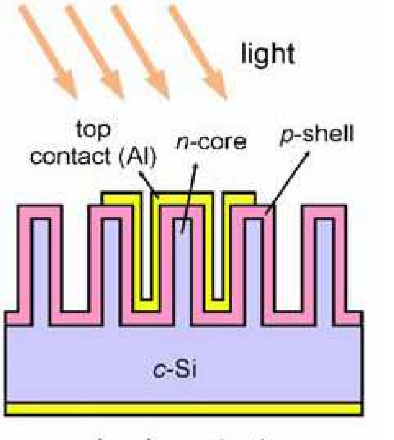


[Garnett09]



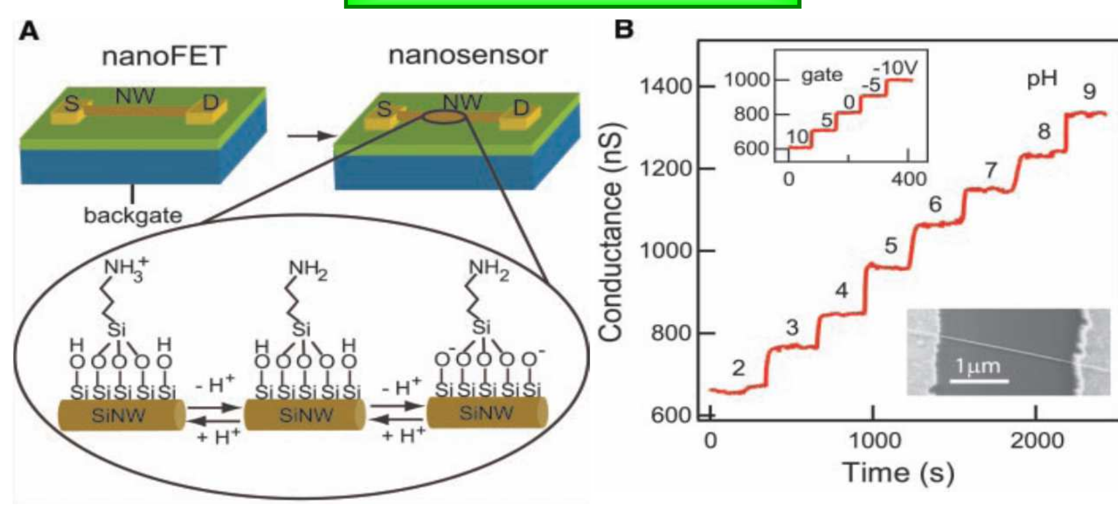
[Schmidt06]

Solar cells



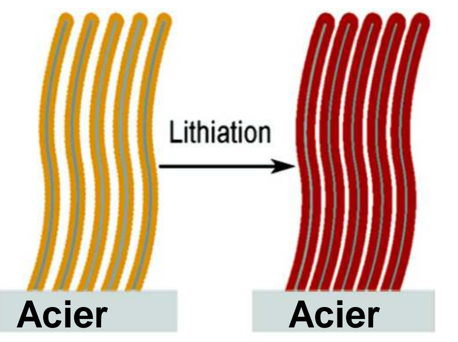
[Gunawan09]

Sensors



[Cui01]

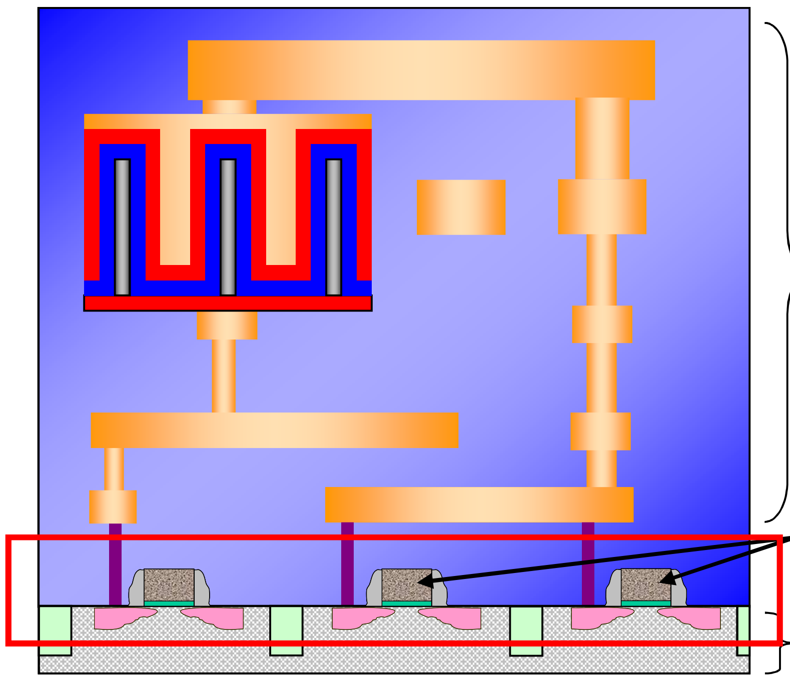
Batteries



Lithiation of Si crystalline-amorphous core-shell nanowires

[Cui08]

Nanowires for nanoelectronics



IC cross section picture

❖ FET in Front End ?

➢ Precise dimensions

➢ Agressive performances

➢ No metallic contamination

⇒ Low interest for CVD VLS NWs

❖ FET in back-end?

➢ Metallic contamination allowed

➢ Cristalline growth on metal

⇒ Challenge (1 NW – 1 device)

❖ High density capacitors in Back End ?

➢ Use the high surface area available from an assembly of NWs

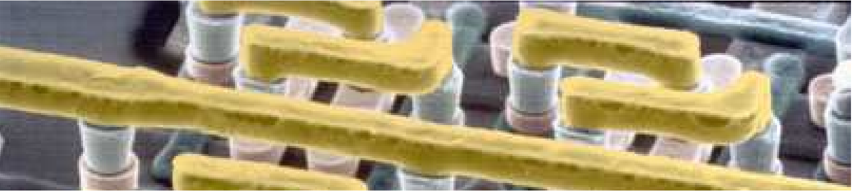
$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot S}{e}$$

⇒ Challenge

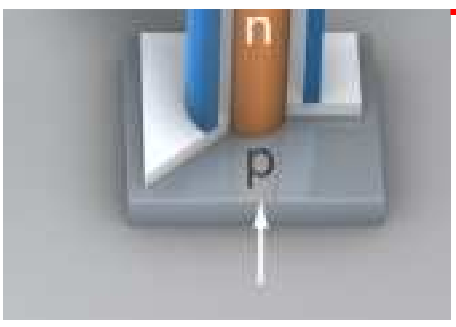
Vertical NWFET

- Gate all around
  - Improve electrostatic control
- Compact
- Integration in interconnection lines

$$C = \frac{S\varepsilon_{ox}}{e_{ox}}$$



Reconfigurable interconnection



TFETs

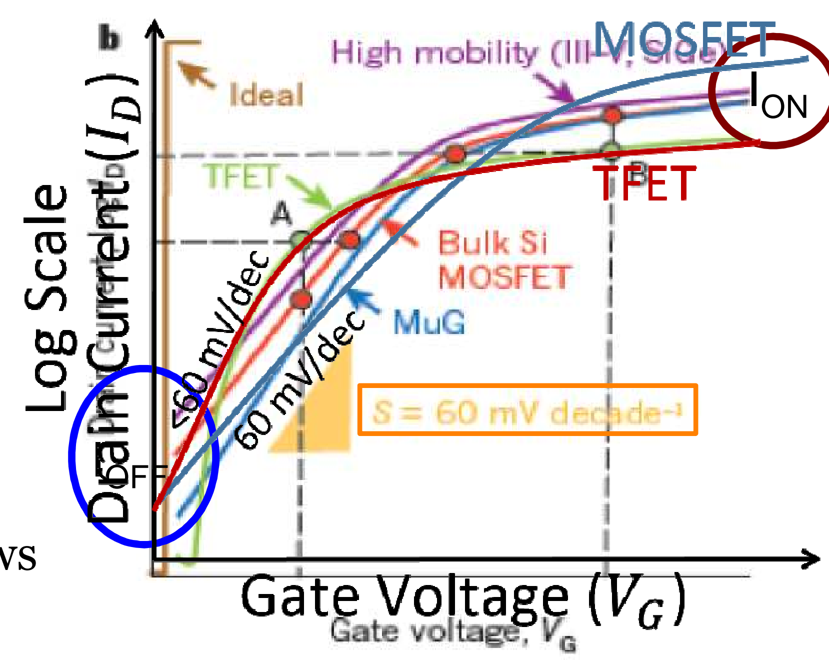
- CMOS subthreshold swing (SS): limitation

$$\frac{k_B T}{q}\ln(10) \sim 60\text{mV/dec at } 300\text{K}$$

  - Scaling down of supply voltage increases the leakage current of MOSFETs (I_{OFF})

Increased power consumption

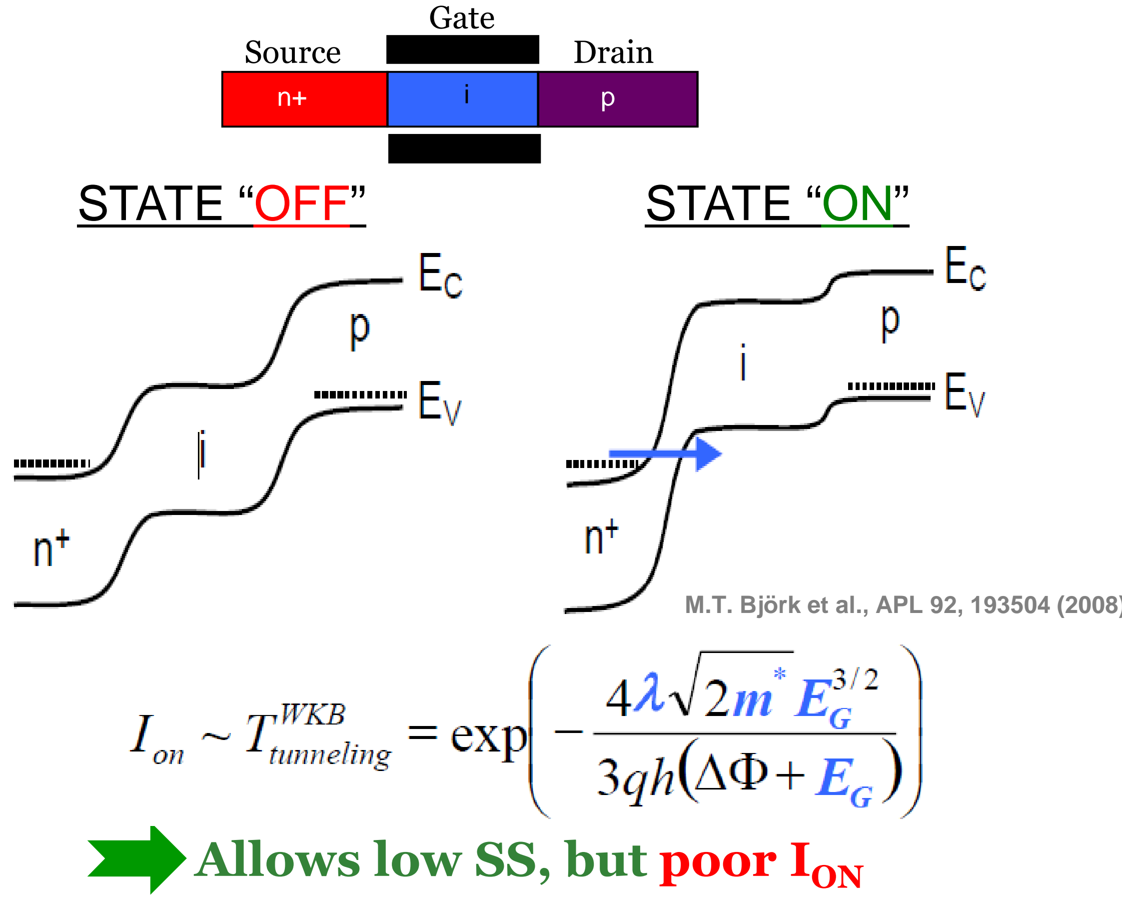
- Interest of steep slope devices. It allows
  - -Low threshold voltage
  - -Low I_{OFF}



Potential candidate: Gate all around vertical Tunnel FET

Introduction: TFETs

- TFET is a reverse biased p-i-n gated diode
- The gate voltage V_G modifies channel E_C and E_V enabling **tunneling** at source/channel junction



$$I_{on} \sim T^{WKB}_{tunneling} = \exp\left(- \frac{4\lambda\sqrt{2m^*}E_G^{3/2}}{3qh(\Delta\Phi + E_G)} \right)$$

Allows low SS, but poor I_{ON}

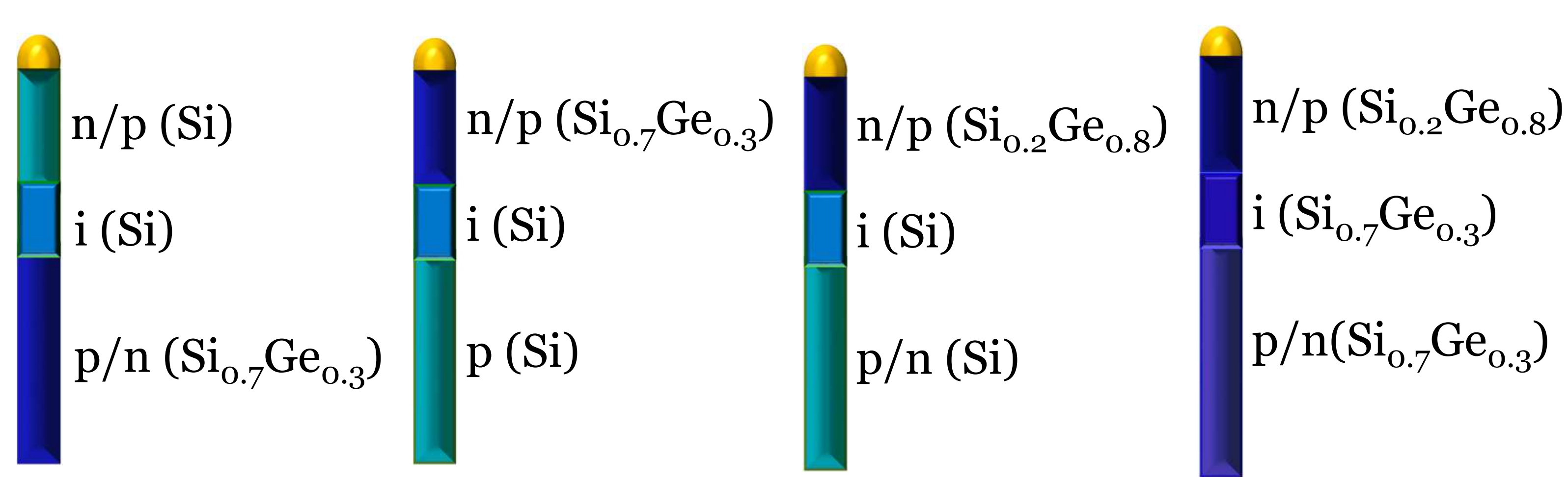
LTM
LABORATOIRE DES TECHNOLOGIES DE LA MICROÉLECTRONIQUE

TFET heterostructures in NWs

Prerequisites for TFET material

- **Low Eg (source) and wide Eg (drain)**
- **Abrupt source-channel junctions**
- **High source doping**

Proposed TFET structures



How to grow Si-SiGe NWs

A. TOP DOWN METHOD

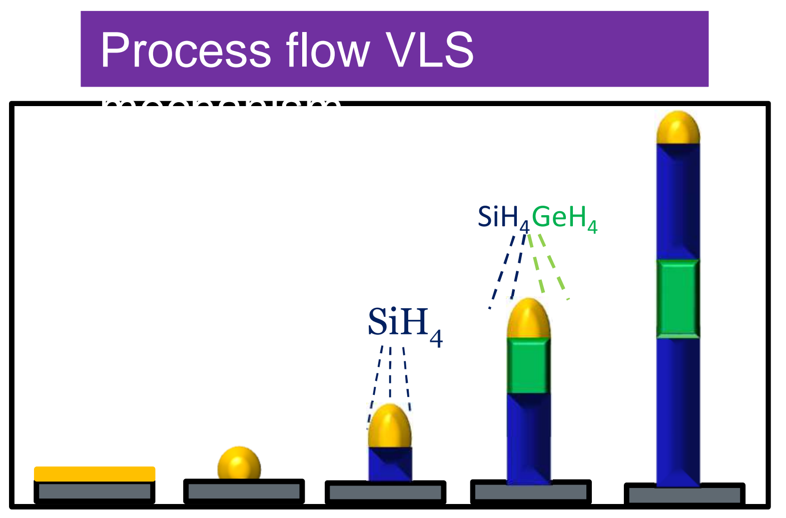
- **Deposition of Si-SiGe multilayers+Etching**

?? Strain relaxation, roughness, defects

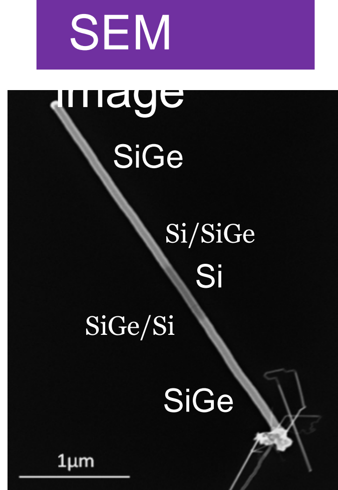
B. BOTTOM UP METHOD

- **Vapor Liquid Solid mechanism (CVD, MBE, Solid phase synthesis..)**

Process flow VLS



SEM



CVD-VLS mechanism allows

- strain relaxation
- low defects

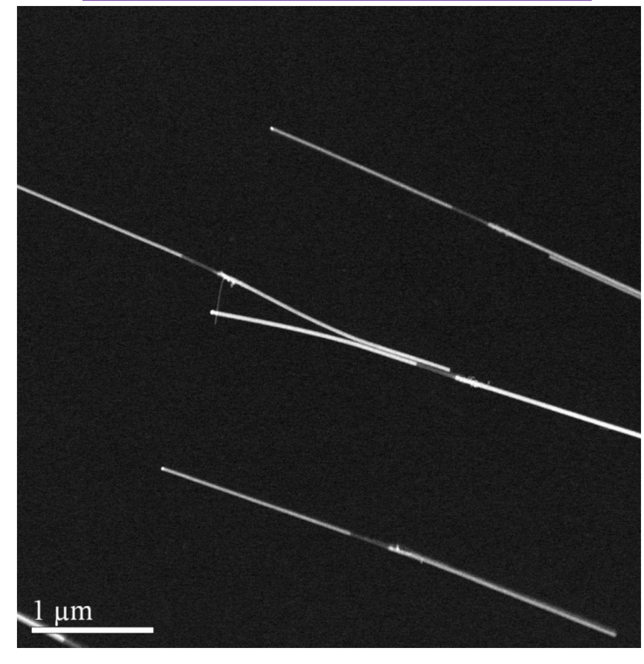
CVD Equipment

RP-CVD reactor

SiNaPs/CEA/INAC/LTM

- **Gas sources** : SiH_4, GeH_4, HCl, H_2, PH_3 (**n type**), B_2H_6 (**p type**)
- **Temperature** : up to 1100° C
- **Pressure** : from 1 to 10 torr

HAADF-STEM image



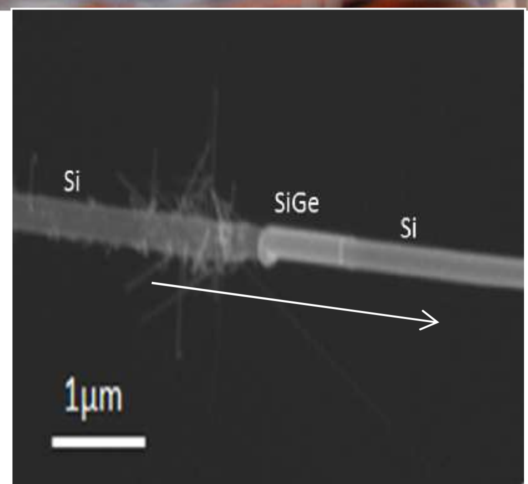
P. Periwal, PhD 2014

Effect of temperature on NW morphology

n ($Si_{0.3}Ge_{0.7}$)

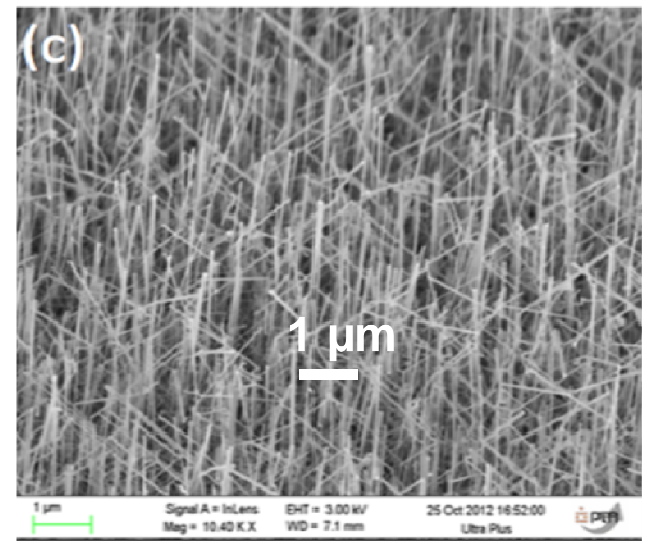
i (Si)

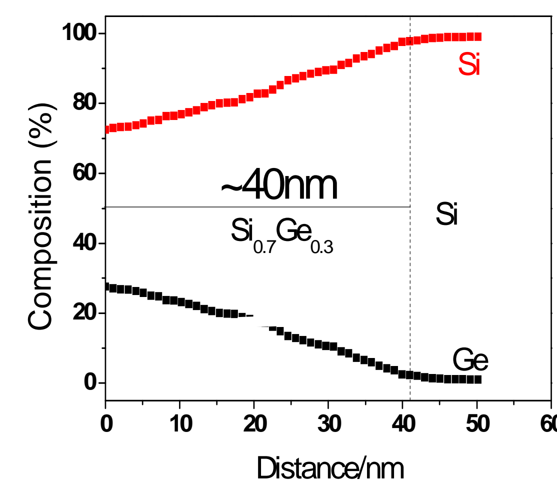
p (Si)



- T_G for Si= 600°C
- T_G for SiGe=450°C

Growth of Si and SiGe at two different temperatures are not favourable





Growth of both segments at 450°C produces high density of NWs

Effect of growth stop on NW morphology

1 min (a) 2 µm

(b) 2 min 2 µm

(c) 3 min 2 µm

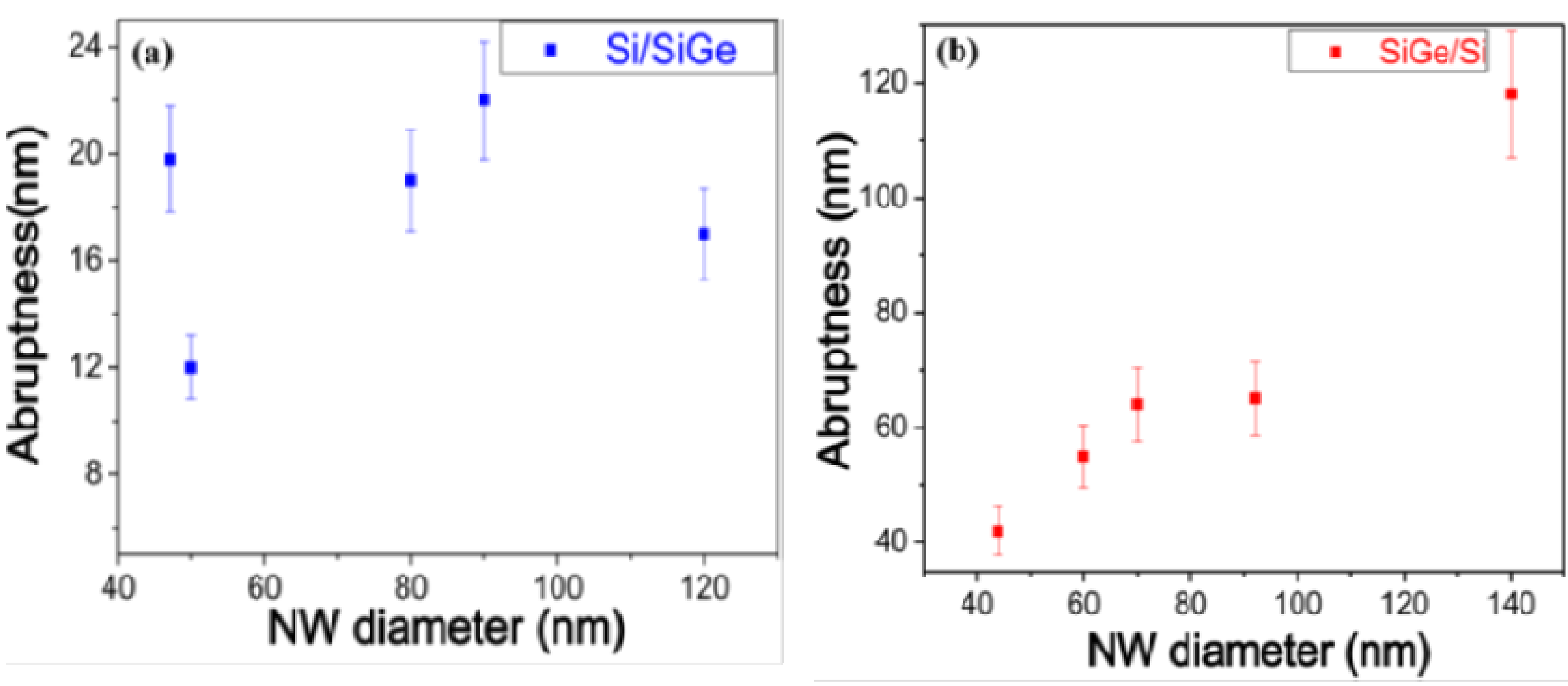
Composition (%) vs. Distance (nm): Ge, Si; Si, ~20nm, SiGe; P= 4.5 Torr

- Growth stop stabilizes the catalyst droplet and improve abruptness.
- It should be for optimum time.
- Destabilization in the droplet induces kinks or twin boundary.

P. Periwal et al JVST A 32 (3) 031101 (2014)

Effect of NW diameter on Si/SiGe and SiGe/Si interface

For x=30% and D=40-120 nm



- $Si_{0.7}Ge_{0.3}/Si$ interface: linear relation
- $Si/Si_{0.7}Ge_{0.3}$ interface abruptness does not exceed 30 nm.

P. Periwal et al NanoLetters 14, 5140 (2014)

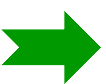
Effect of Ge composition in $Si_{1-x}Ge_x$ part (0.3<x<0.8)

In collaboration with Gilles Patriarche, LPN-Paris

$Si_{0.4}Ge_{0.6}$-Si-$Si_{0.4}Ge_{0.6}$ for D=50-60 nm

(b)
SiGe
Si
SiGe
200 nm

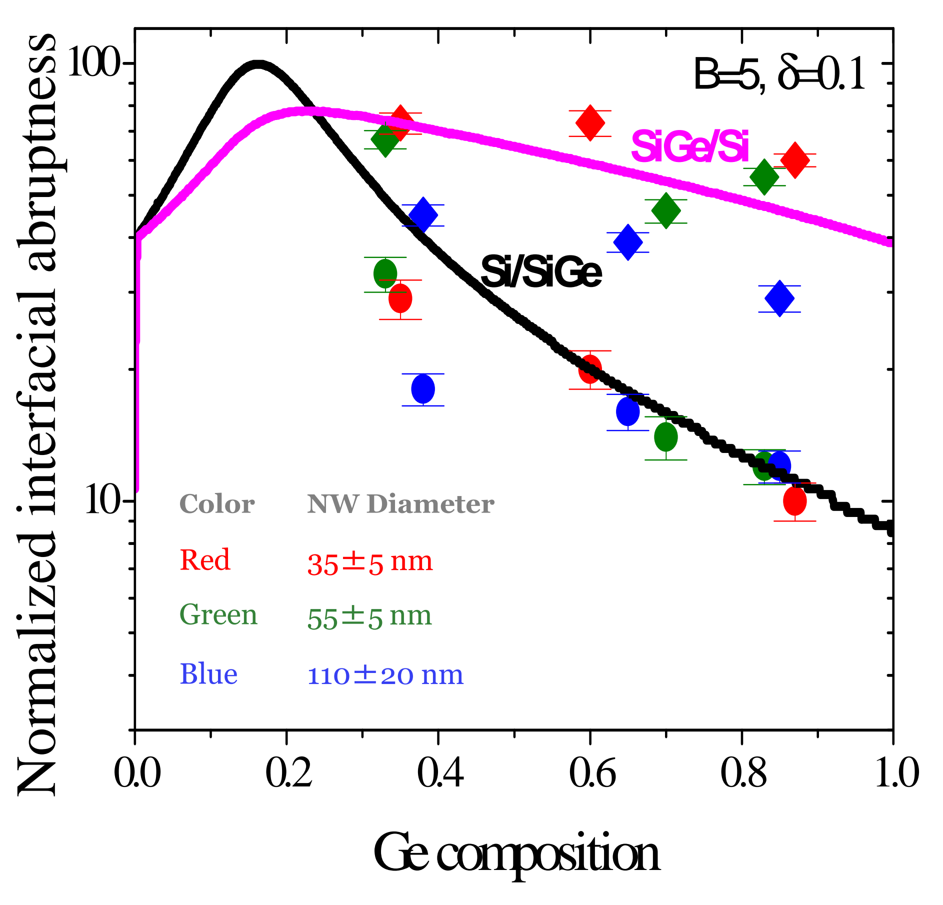
55 nm
16 nm
Distance (nm)



Asymmetric heterointerfaces: $Si_{1-x}Ge_x$/Si is always broader than Si/$Si_{1-x}Ge_x$

P. Periwal et al NanoLetters 14, 5140 (2014)

Modeling & Experimental results

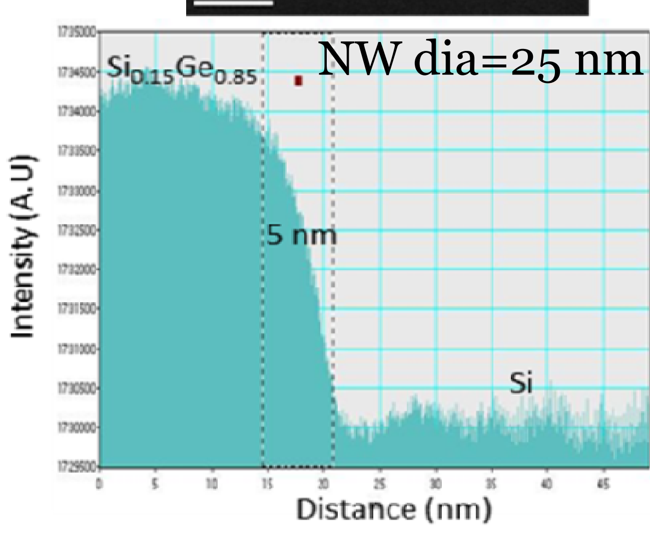


Si/SiGe interface

$Si_{0.15}Ge_{0.85}$

Si

20 nm



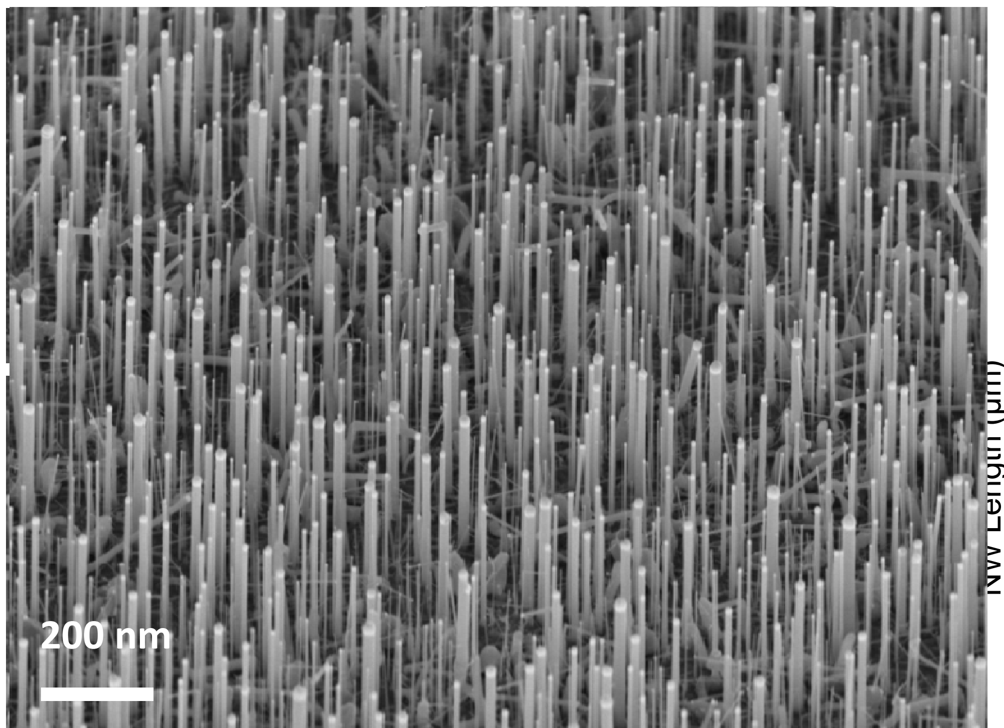
- Experimental data fits well with the Model
- High Ge & small dia = sharp Si/SiGe interface

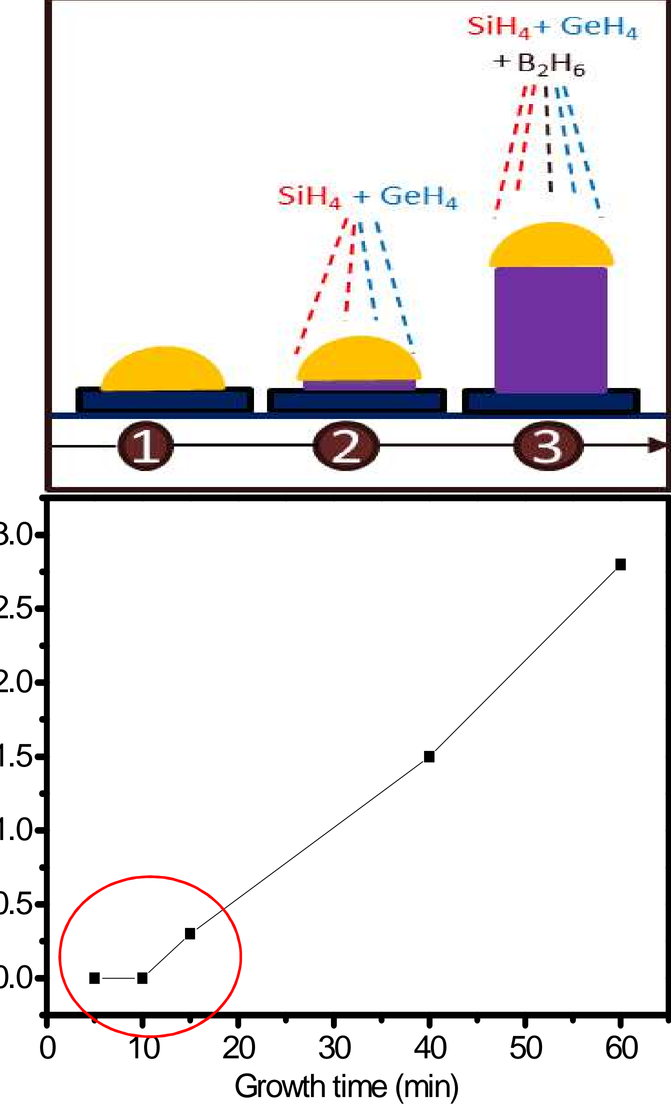
P. Periwal et al NanoLetters 14, 5140 (2014)

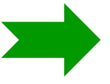
Two step growth process: B doped $Si_{0.7}Ge_{0.3}$ NWs

Two step process:

- Continuous flow of SiH_4, GeH_4 and HCl but no exposure of diborane for few minutes.
- Introduction of diborane gas






No growth occurs during first 5 minutes

Passivation effect by PH_3 in Ge NWs: Modeling

1 (0.5 nm/min)

2 µm

2(0.5 n

N+/n junctio

1µm

2 µm

2 µm

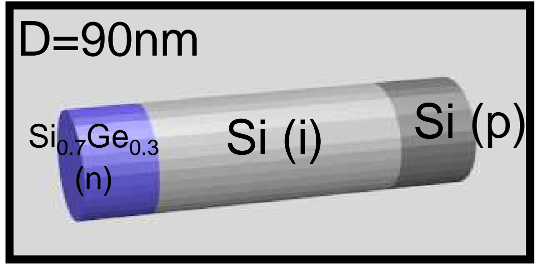
anism which takes place

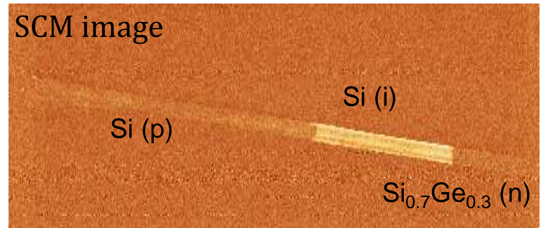
e.

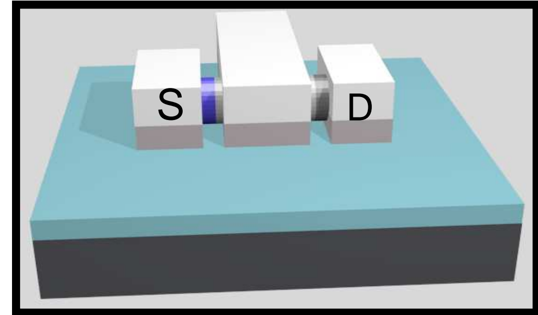
- Mechanism~MBE occurs.

P. Periwal et al APL Mat 2 046105 (2014)

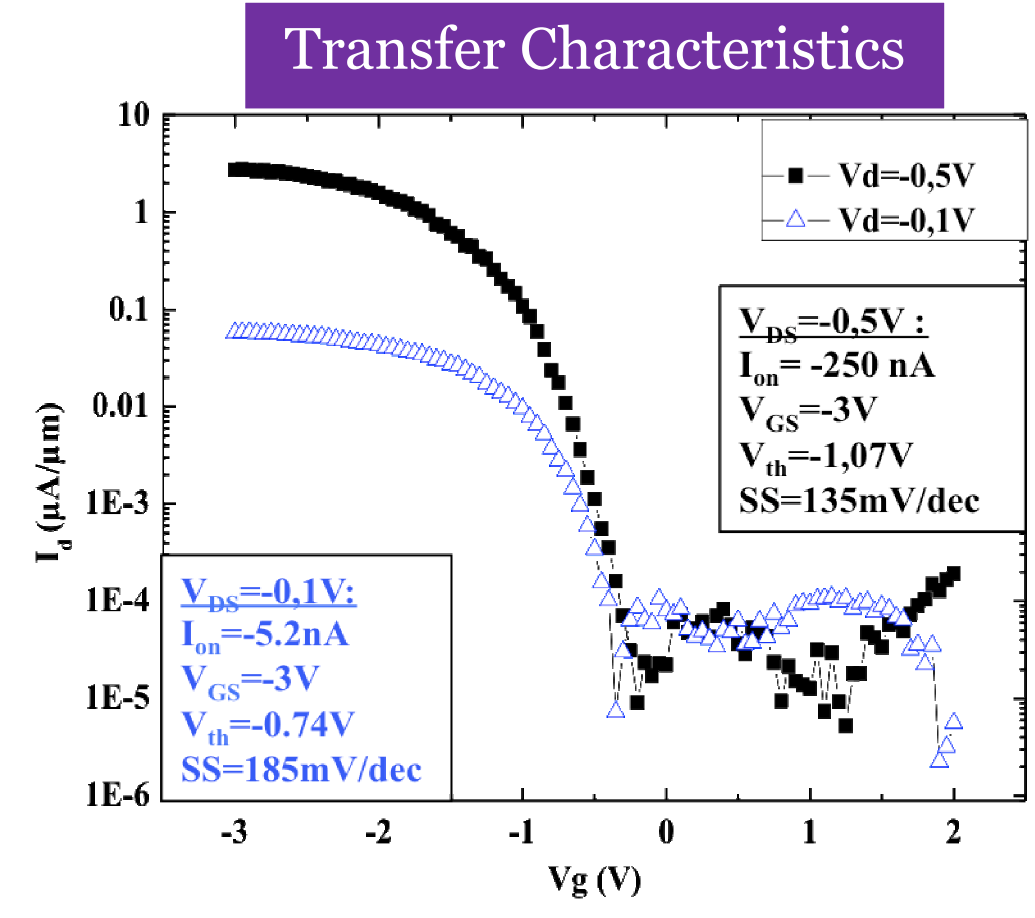
Perspectives: Integration of heterostructure NW in TFET







Device in Ω Gate configuration



Horizontal p-Si/i-Si/n-$Si_{0.7}Ge_{0.3}$ axial heterostructure nanowire Tunnel FET using Al_2O_3 as gate dielectric represents SS = 135 mV/dec at V_{DS}=-0.5 V

Thesis Virginie Brouzet (LTM/IMEP) 2015

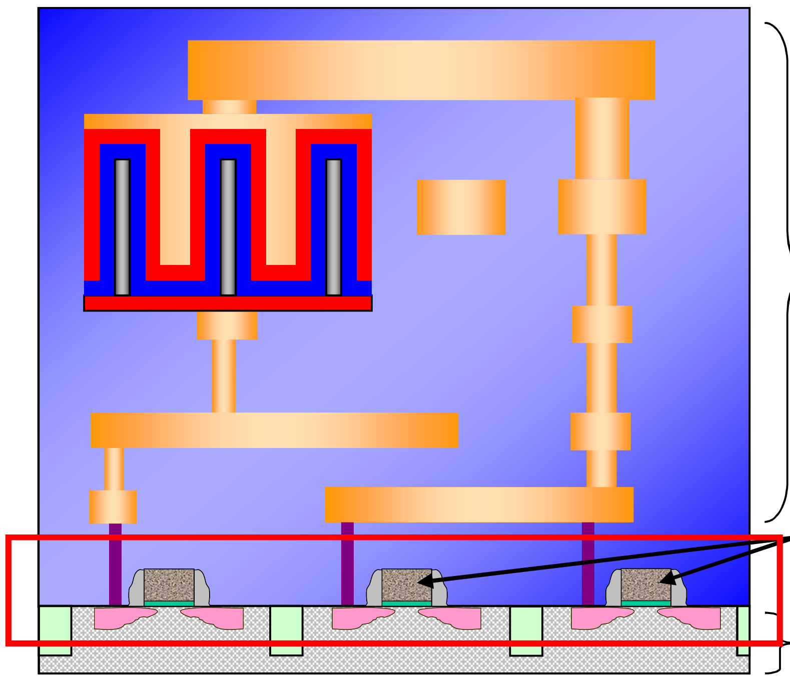
OUTLINE

- Nanocrystals for memory devices

- Nanowires for low power devices, capacitors and sensors
  - Low power devices
  - MOS and MIM capacitors
  - Sensors

- SiGe and InGaAs thin films for NMOS and PMOS FET

Nanowires for nanoelectronics



IC cross section picture

❖ FET in Front End ?

➢ Precise dimensions

➢ Agressive performances

➢ No metallic contamination

⇒ Low interest for CVD VLS NWs

❖ FET in back-end?

➢ Metallic contamination allowed

➢ Cristalline growth on metal

⇒ Challenge (1 NW – 1 device)

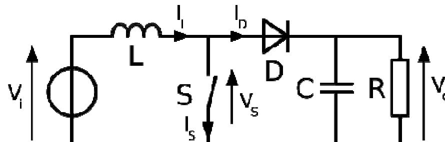
❖ High density capacitors in Back End ?

➢ Use the high surface area available from an assembly of NWs

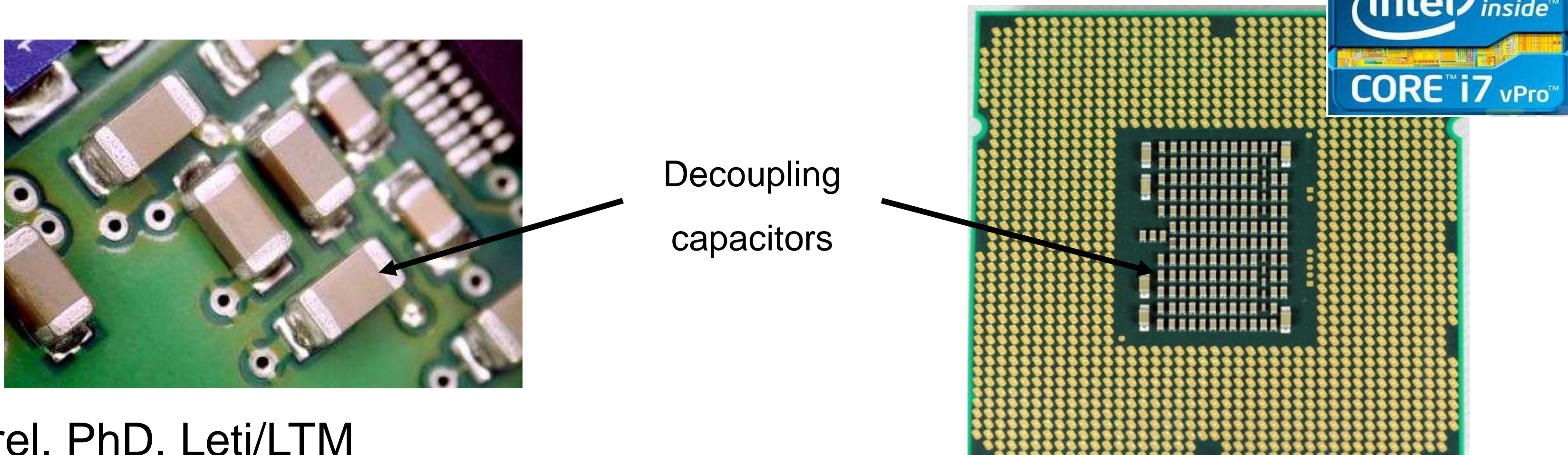
$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot S}{e}$$

⇒ Challenge

High capacitance density devices



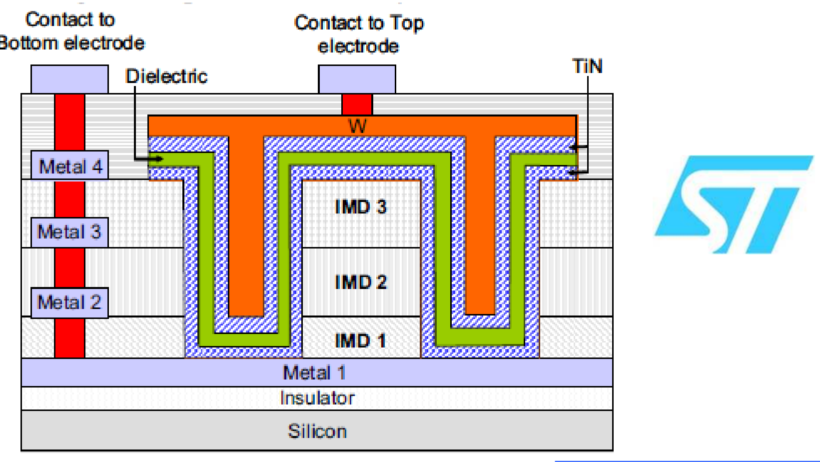
- DC/DC convertor
- **Decoupling capacitor** is a capacitor used to decouple one part of an electrical network (circuit) from another. Noise caused by other circuit elements is shunted through the capacitor, reducing the effect it has on the rest of the circuit.
  - ✓ high capacitance value (1 nF - 1 µF)
  - ✓ Low leakage current
  - ✓ High breakdown voltage (> 10 V)
  - ✓ Low series resistance



PH Morel, PhD, Leti/LTM

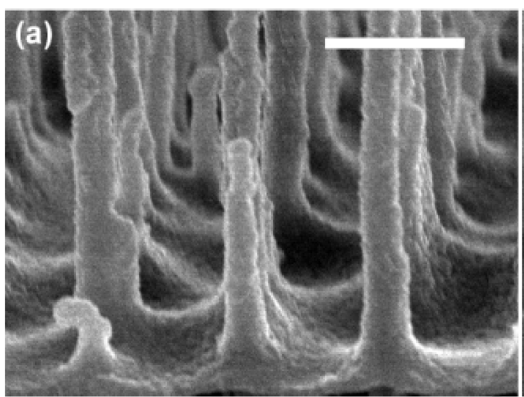
Technologies for high density capacitors

Back-End



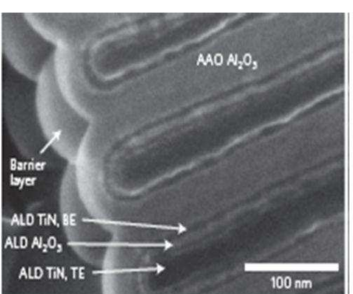
A. Bajolet *et al*, ESSDERC (2005)

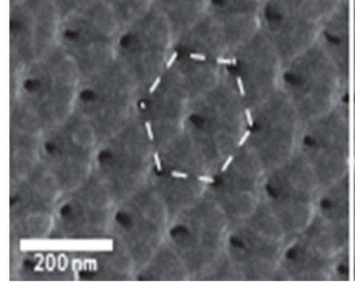
C ~ 4,5 µF/cm²
J ~ qq nA/cm² à 1V



C ~ 0.62 µF/cm²
J ~ 5 µA/cm² à 1V

Choi *et al,* Diamond & Related Materials (2009)

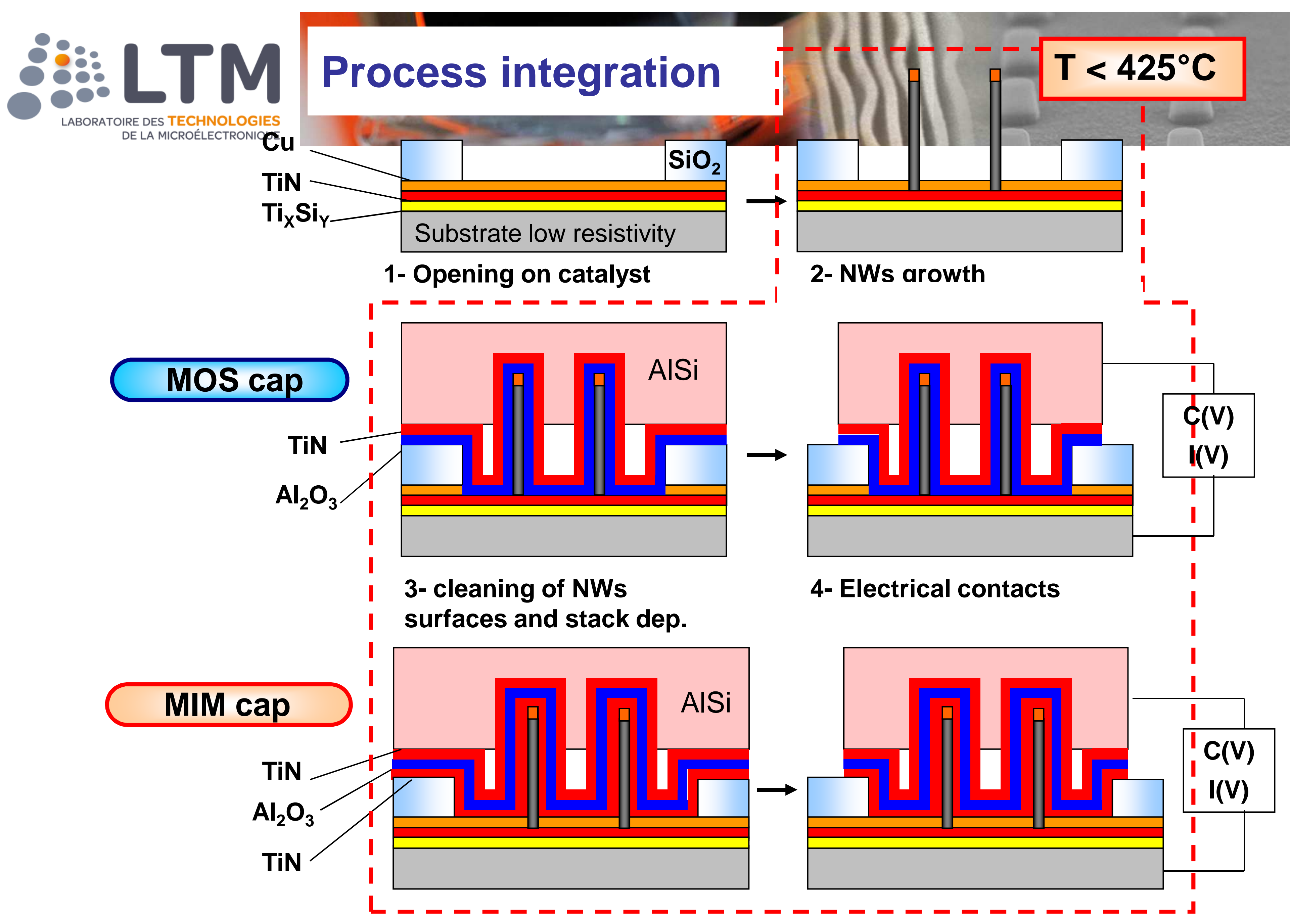




P. Banerjee *et al*, Nat. Nanotech. (2009)

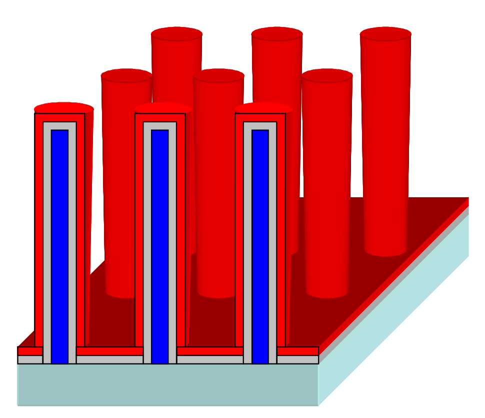
Frequency = 20 Hz

C ~ 100 µF/cm²
J ~ 5 nA/cm² à 2V



T. Ernst et al., CEA-Leti

Process integration



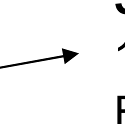
Materials choice

- **Dielectric** : ALD alumina
  - ✓ Conformal deposition
  - ✓ high-κ, $\varepsilon_r = 9$
  - ✓ High breakdown voltage : 7-10 MV / cm
  - ✓ Large band gap : 8,7 eV

- **Electrodes** : CVD - TiN
  - ✓ Conformal deposition
  - ✓ Thermodynamically inert with alumina
  - ✓ High workfunction : 4,8 eV
  - ✗ High resistivity > 200 μΩ.cm
    - ➪ put AlSi for top electrode (2,7 μΩ.cm)

Requirements

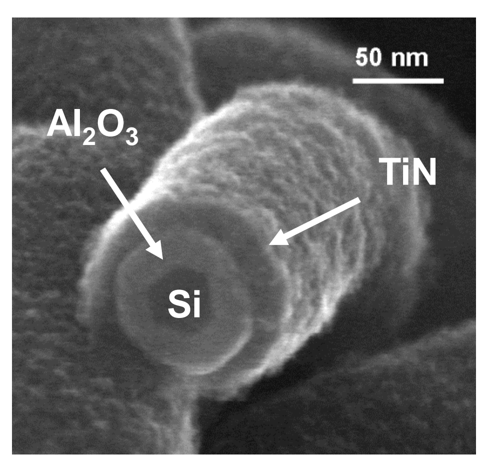
- High capacitance density
- Low serie resistance

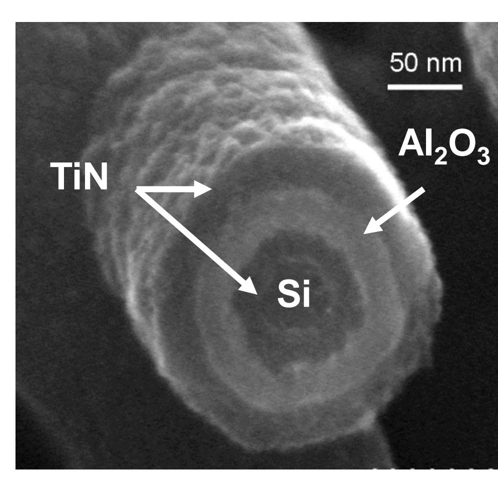


S = 10 000 μm²
10 < C < 20 μF/cm²
R_S ~ 6 Ω (MIM) et R_S ~ 8000 Ω (MOS)

Morphological characterization

- TiN, 20 nm conformal
- Al_2O_3, 20 nm conformal





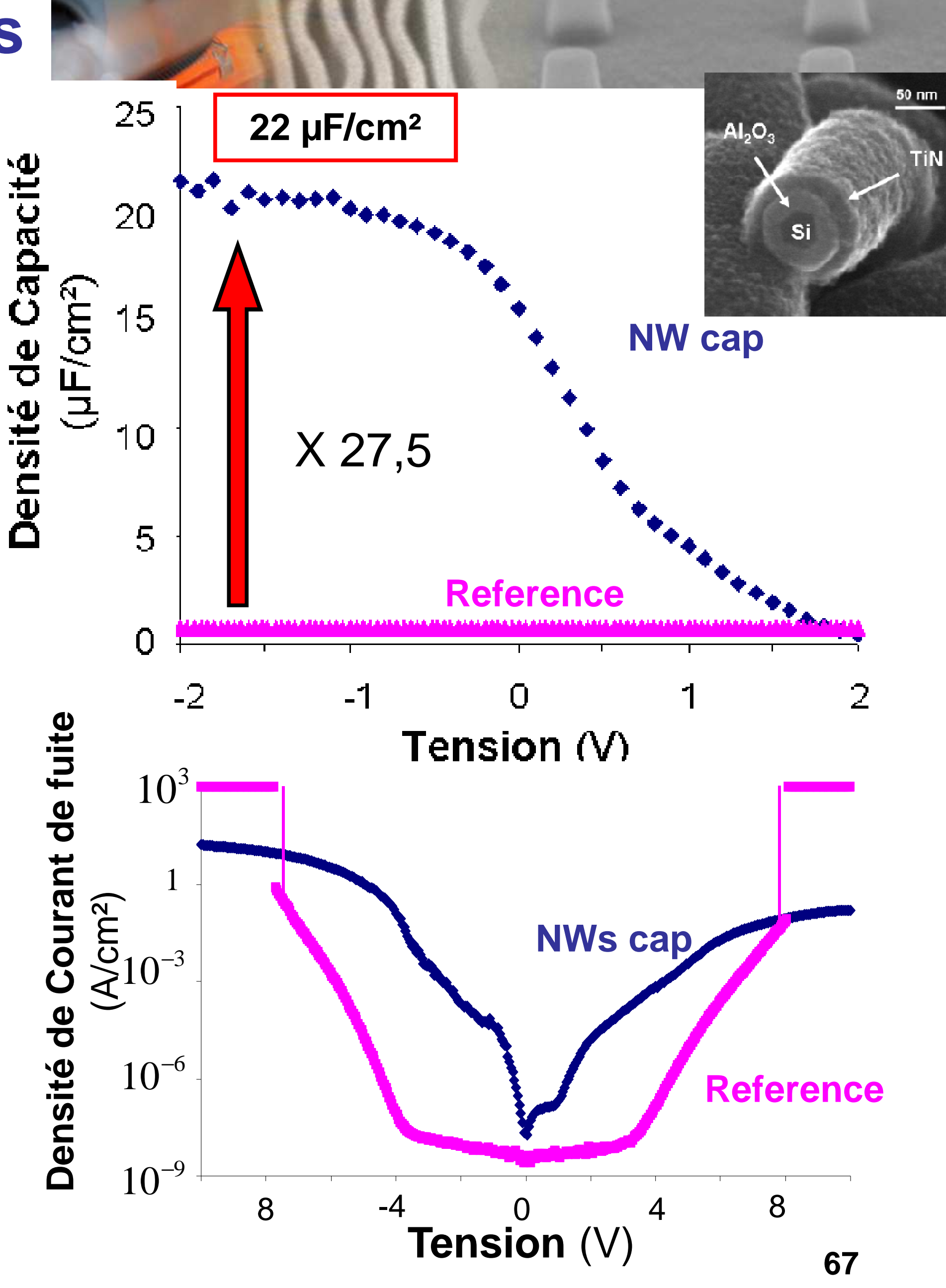
SEM cross section

MOS capacitors

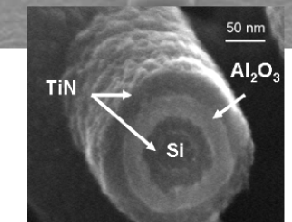
High capacitance density

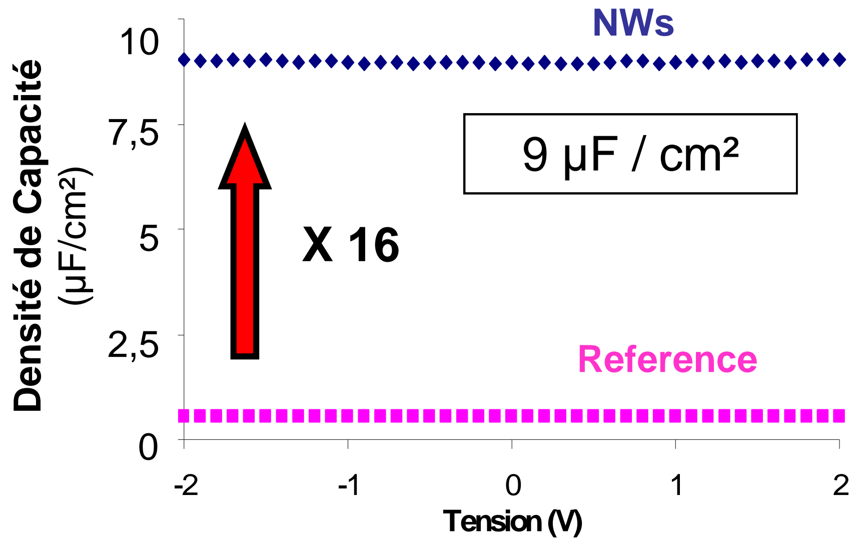
- 10 nm alumina
- SI NWs surface cleaning and passivation before ALD deposition

- leakage for NWs capacitors
  - NWs : 49 µA/cm² à -1V
  - Reference : 6,3 nA/cm²
- Lower breakdown voltage



MIM capacitors





C(V) @ 20 Hz with 15 nm d'alumine

- Gain in capacitance : 16
- decrease of the capacitance from 20 Hz
  - → High serie resistance
  - → Technological parameters to control

Summary

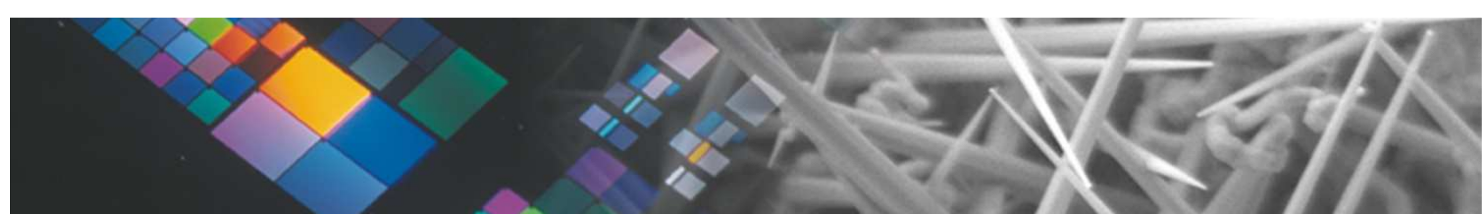
References	[Black04] **Gravure**	[Choi10] **Nanotubes**	[Banerjee09] **Alum. nanop**	**Al_2O_3 15 nm**
Density of Capacitance (µF/cm²) F	3,13	0,62	10	**9,6**
Density of leakage current de fuite à 1V (nA/cm²) A	2 500	5 000	5	**11**
(F/A)	1,25	0,124	2000	**873**

Industrial requirements for DC/DC converter and decoupling capacitors

	I / C @ 3,6 V	Breakdown V
Specifications Ipdia	< 7 x 10^{-12} A / nF	> 10 V
NW cap 15 nm Al_2O_3	3,5 x 10^{-11} A / nF	9 V

OUTLINE

- Nanocrystals for memory devices
- Nanowires for low power devices, capacitors and sensors
  - Low power devices
  - MOS and MIM capacitors
  - Sensors
- SiGe and InGaAs thin films for NMOS and PMOS FET



Silicon nanonets, Sensors

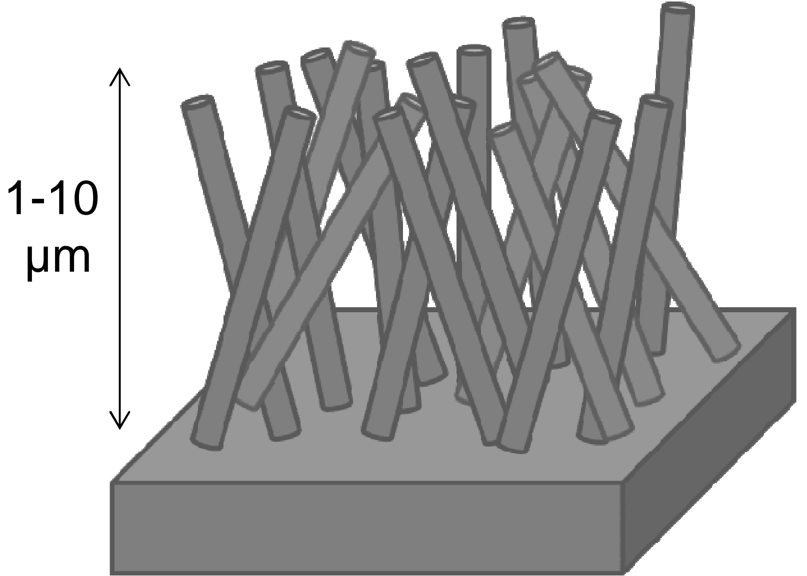
P. Serre, PhD 2014

UNIVERSITÉ DE GRENOBLE

Nanonets

Nanonet = NANOstructured NETwork
Network of 1D (NFs or NTs) randomly oriented

3D Nanonets
thickness ≤ length



2D Nanonets
thickness << length

10-100
nm

Introduction : Si 2D nanonets

Characteristics

- High aspect ratio
- High specific area

- Electrical conductor
- Optical transparency

- Mechanical flexibility
- Functionnalisation possible

- Versatile
- Reproductible

Applications

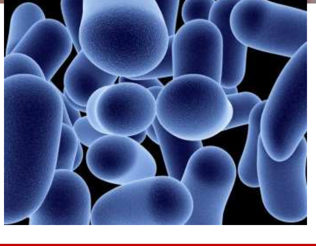
- Conductive, transparent, flexible electrodes,
  - → Solar cells
  - → OLED
  - → touch screen

- Photodetection

- Chemical and biological sensors

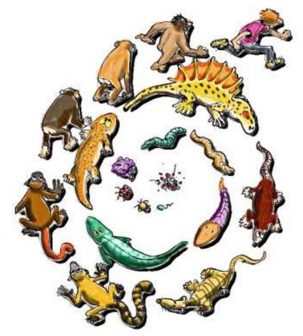
Si Nanonets for detection

Challenges



Health
Medical diagnostic

Evolution



Sensors

Environnement
Water analysis

Agroalimentaire
Bacteria detection

→ Portable
→ Reliable
→ Low cost
→ Fast response

Nanonets fabrication by filtration method

NWs elaboration

P. Periwal (LTM) — NW Si-VLS (100 nm, 2 µm)

M. Martin (LTM) — NW Si-etching (1 µm)

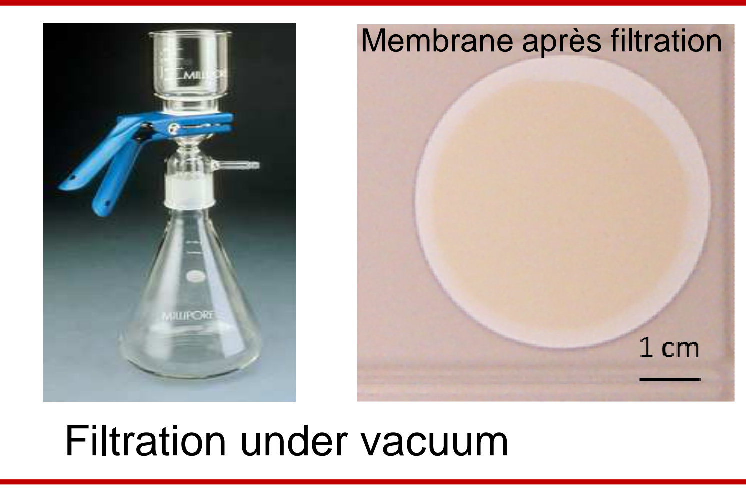
Sonication

Solution

NW concentration monitoring by absorbance spectroscopy

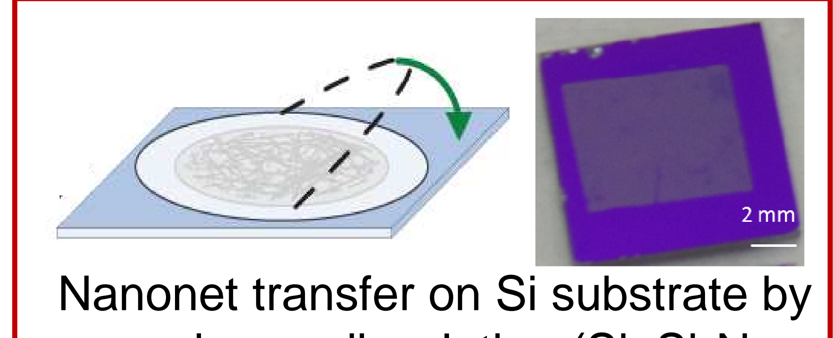
Filtration

Nanonet fabrication



Filtration under vacuum

Transfert on substrate



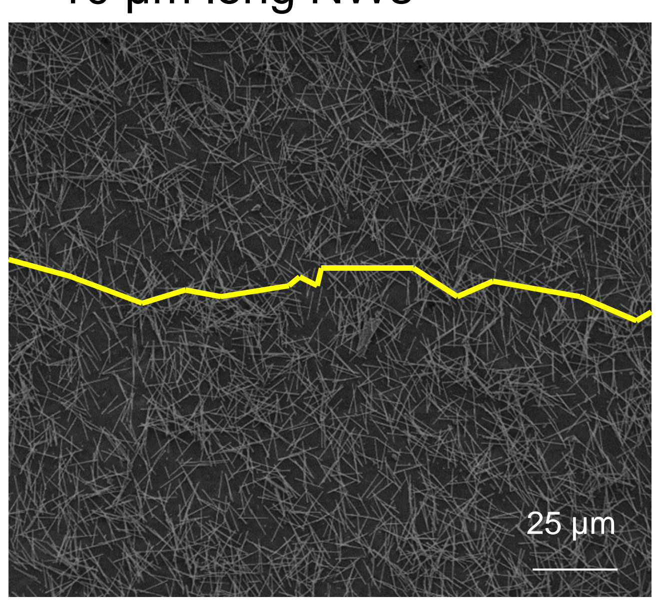
Nanonet transfer on Si substrate by membrane dissolution (Si, Si_3N_4, SiO_2, PE …)

Simple, low cost
RT process
Limited thickness
Large scale

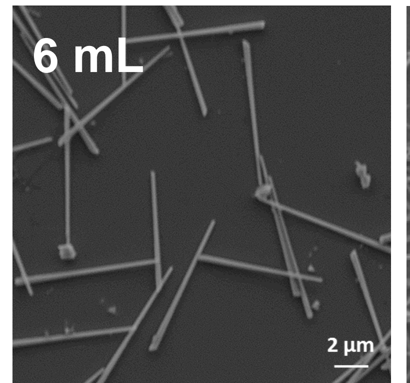
C. Ternon et al., LTM-LMGP

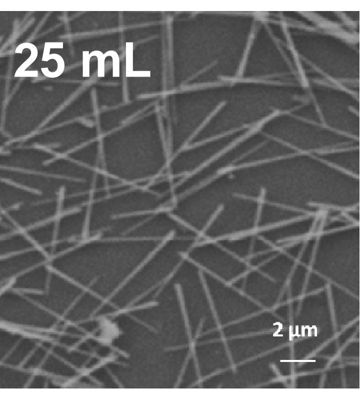
Nanonet morphology

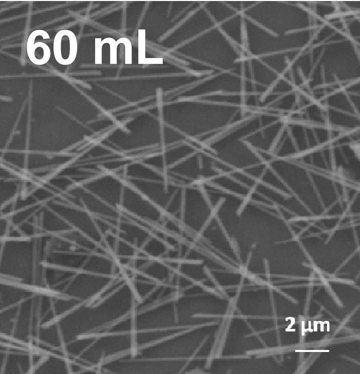
10 µm long NWs

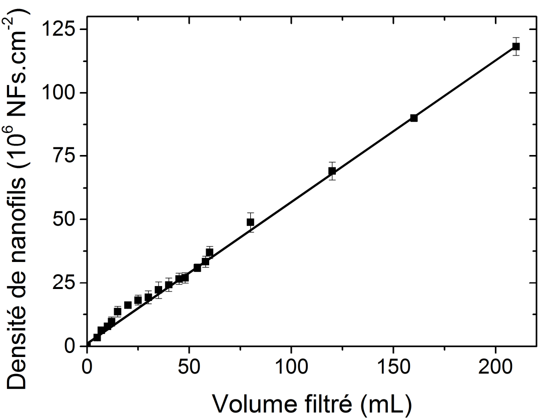


Randomly oriented
Well interconnected
Percolation path
Uniform
Large scale
Good adherence with substrate



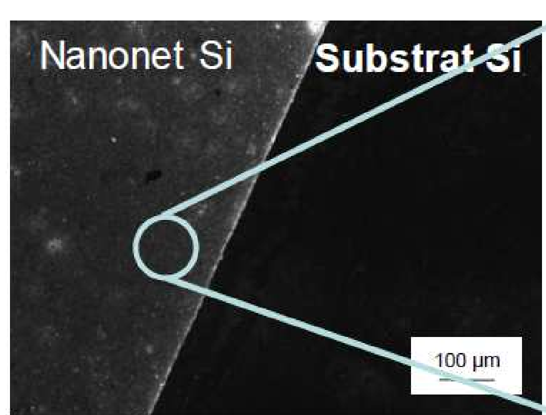


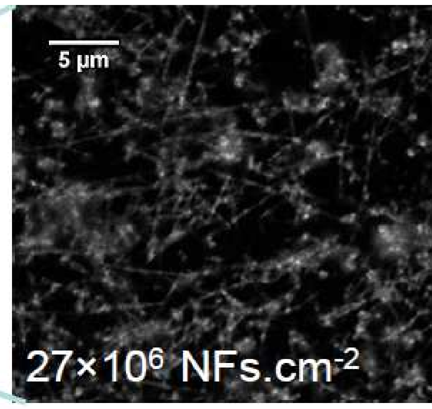




Precise control of NWs density

ADN hybridation detection by fluorescence

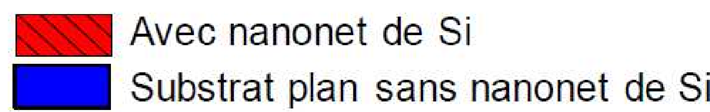


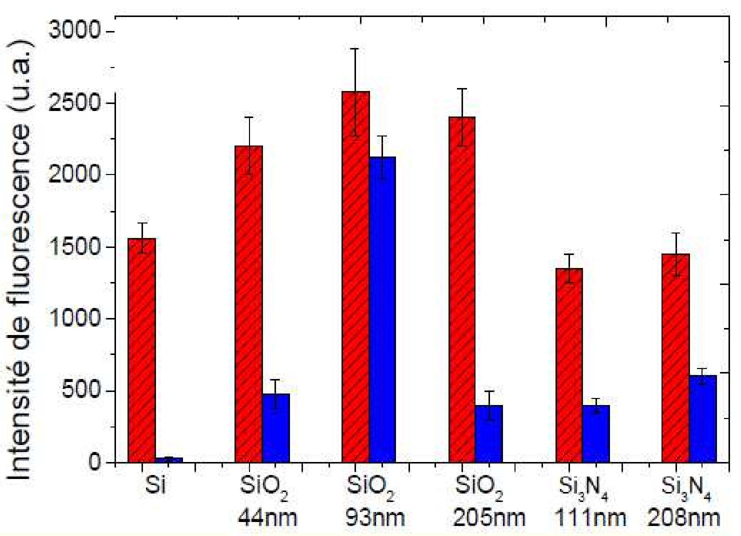


Fluorescence sur les nanonets de Si

Signal de fluorescence discret

P. Serre et al,
Sensors and Actuators B, 182, 390-395 (2013)





Détection de l'ADN par fluorescence
Immobilisation de l'ADN sur les nanonets de Si

Signal dépend du substrat
Amélioration du signal sur les nanonets de Si par rapport à tous les substrats plans

Si Nanonets DNA sensors

Sensibility

Intensité de fluorescence (u.a.)
10000
1000
100
10
1
1
10
100
1 000
10 000
Concentration d'ADN cible (nM)
0,1 µM
10 µM

Selectivity

Intensité de fluorescence normalisée (%)
100
75
50
25
0
Ct
1bm
2bm
NonCt
Ct (0bm)
1 bm

Integration in an DNA dye

Nanonet Si
5 mm

P. Serre *et al*,

DNA sensor : sensible, selective.

OUTLINE

- Nanocrystals for memory devices

- Nanowires for low power devices, capacitors and sensors
  - Objective : low power devices
  - Si/SiGe nanowires catalytic growth
  - Other applications

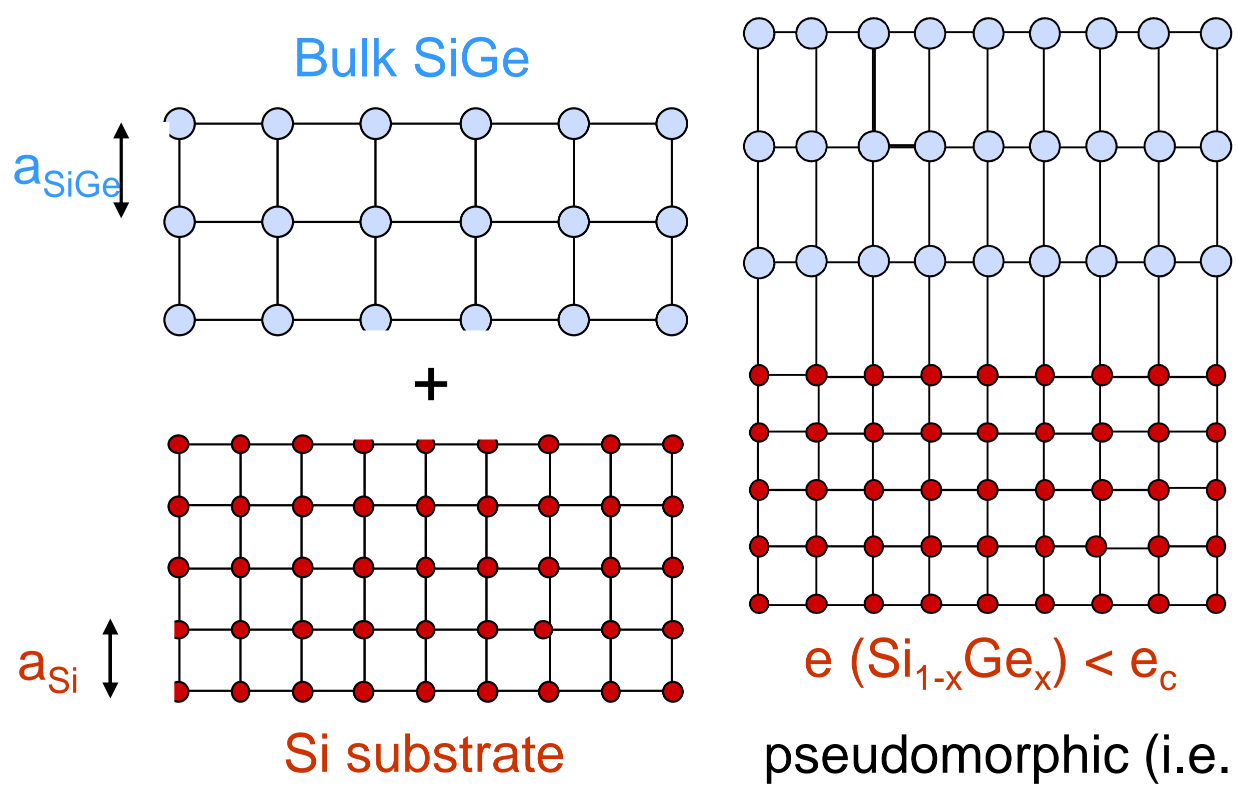
- SiGe and InGaAs thin films for NMOS and PMOS FET

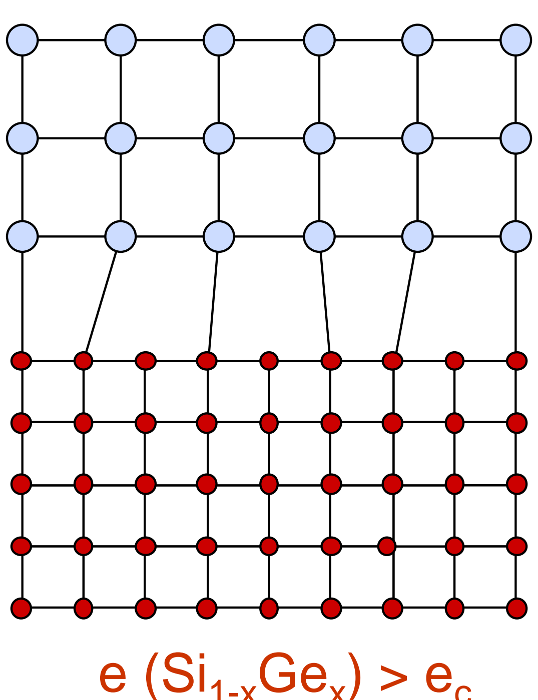
Roadmap of Energy Efficient Devices

Need of SiGe alloys for future devices and III-V exploration on a Si platform

EPITAXY

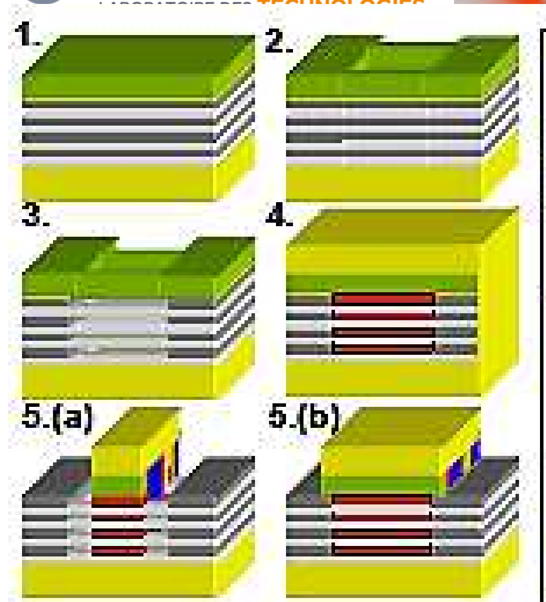
Epitaxy = mono-crystalline layer grown on a mono-crystalline substrate;
homo-epitaxy : layer A (Si) on substrate A (Si);
hetero-epitaxy : layer B (SiGe) on substrate A (Si)
a ($Si_{1-x}Ge_x$) = 5.43105 + 0.20050x + 0.0263x^2 Å > a(Si) = 5.43105 Å =>
Strain accumulation inside the SiGe layer when grown on Si. 2 scenarii :



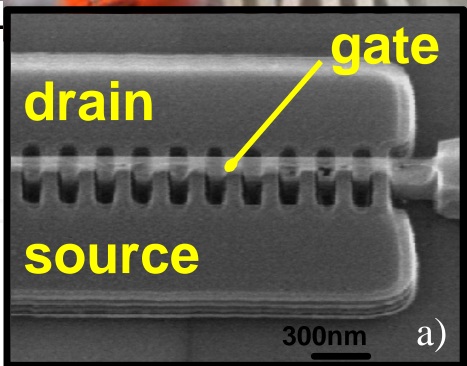


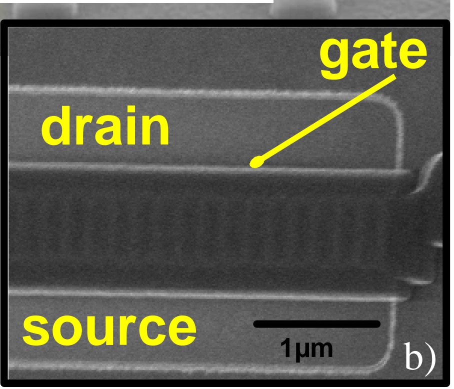
Courtesy of JM Hartmann, CEA-Leti

MULTI-CHANNELS AND 3D NANOWIRES



1. Epitaxy of Si/SiGe superlattice
2. Etching (RIE) of multilayer
3. Selective isotropic etching of SiGe
4. Gate stack definition: HfO_2/TiN/poly-Si CMP poly-Si SiO_2 hard mask
5. Gate etch (anisotropic+isotropic) (a) Etched gate (EG) (b) Plugged gate (PG)





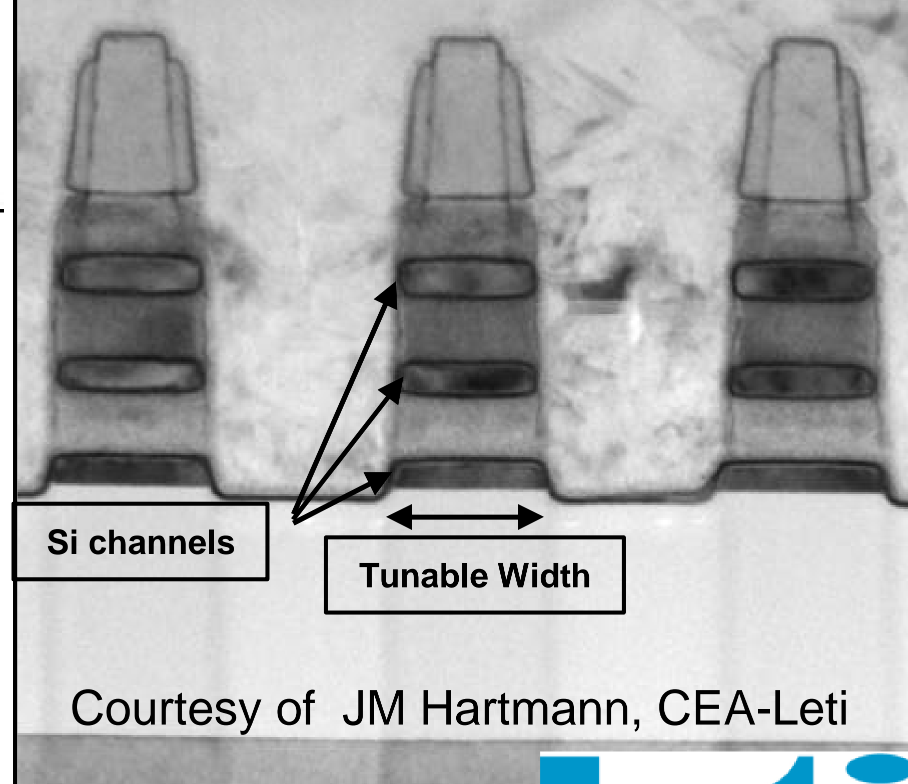
1 - Growth of SiGe/Si superlattices on SOI

2 - Anisotropic etching of those SL

3 - selective plasma etching of SiGe

4 - gate stack formation

5 - gate etch

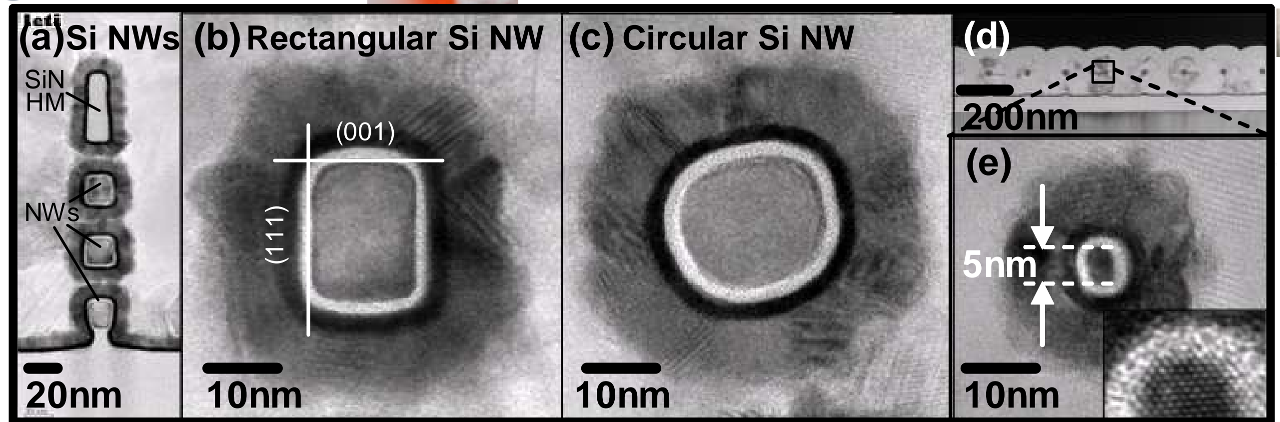


Superior I_{on}/I_{off} trade-offs in MBCFETs :
nMOS : 2.27 mA/µm ⇔ 16 pA/µm
pMOS : 1.32 mA/µm ⇔ 16 pA/µm

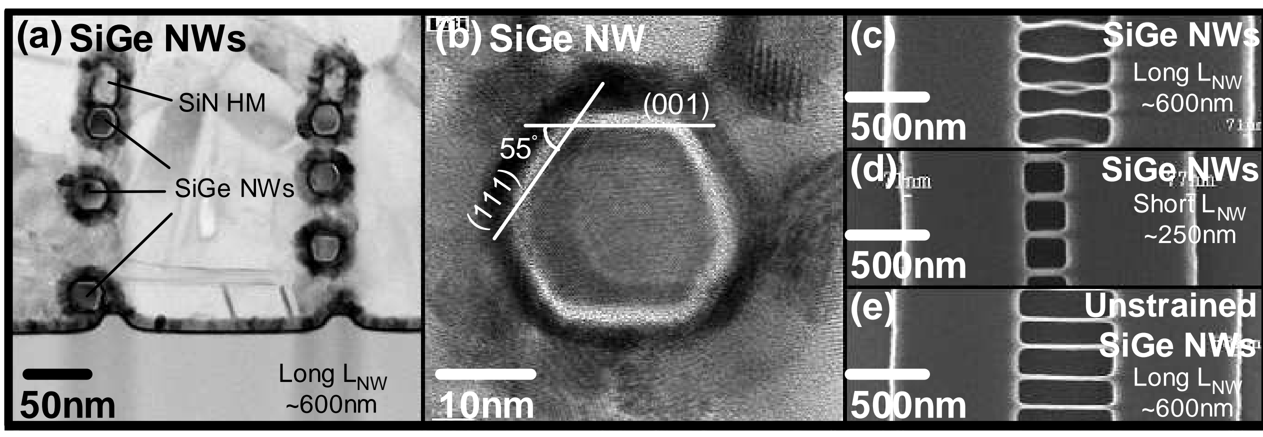
Sol. State Electron. 52 (2008) 519; VLSI Tech. 2008 (16); IEDM 2008 (749)

leti

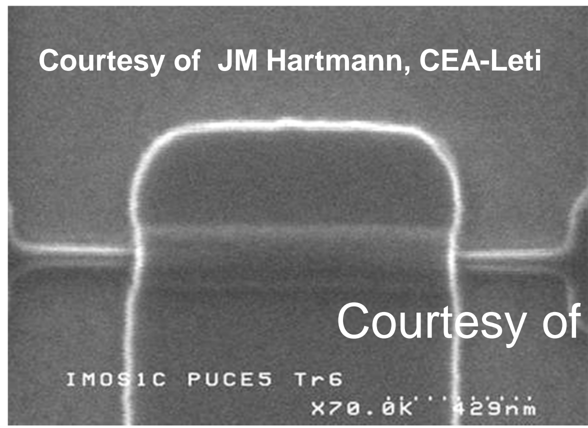
NW ENGINEERING THANKS TO EPITAXY

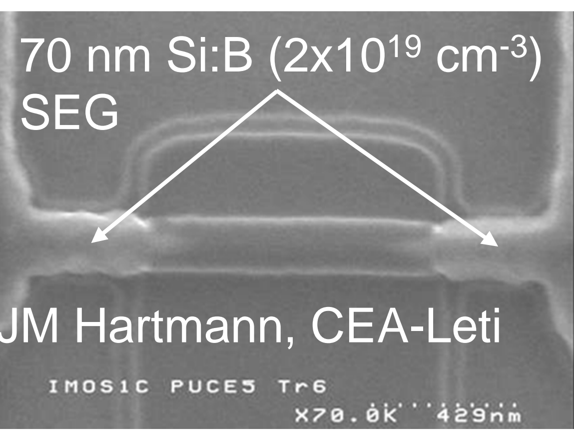


H_2 bake of square-based Si NWs : rounding. Combined with self-limiting oxydation => very small diameter NWs.



H_2 bake of square-based SiGe NWs : hexagonal section. SEG of thin Si cap to improve hole mobility.





Selective thickening of the access regions of Si NWs

APL 91, 233502 (2007); ECS Trans. 13 (1), 195 (2008) & 27 (7) 471 (2009)

III-V properties

Room temperature properties	Si	Ge	GaAs	InAs	InP	InSb
Electron mobility ($cm^2\ V^{-1}\ s^{-1}$)	1 400	3 900	8 500	40 000	5 400	77 000
Hole mobility ($cm^2\ V^{-1}\ s^{-1}$)	450	1 900	400	500	200	850
Bandgap (eV)	1.12	0.66	1.42	0.35	1.34	0.17
Lattice parameter (Å) Diamond or blende-zinc structure	5.431	5.658	5.653	6.058	5.869	6.749

$\Rightarrow$ **Conduction channel (nMOS) : InGaAs ([In] : 30-70%) on GaAs / Ge / Si when thinking of a monolithic integration on Si**

Challenges : Growth of InGaAs channel on Si(100)

- Lattice mismatch (Si-GaAs 4%, Si-InAs 10%)
- Polarity induces antiphase domains
- Thermal expansion coefficient limits the total thickness before cracks appearing

Antiphase domains

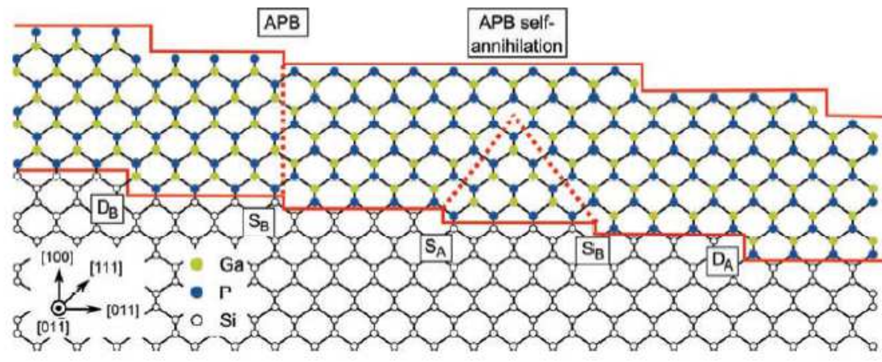


Figure 3: Schematic diagram of the formation of anti-phase disorder due to III-V heteroepitaxy on a Si(100) substrate. Single-layer steps of the Si(100) surface induce anti-phase boundaries (APBs) which penetrate through the film and can be subject to self-annihilation, while double-layer steps on the substrate prevent the formation of APBs during nucleation.

DOESCHER PhD,

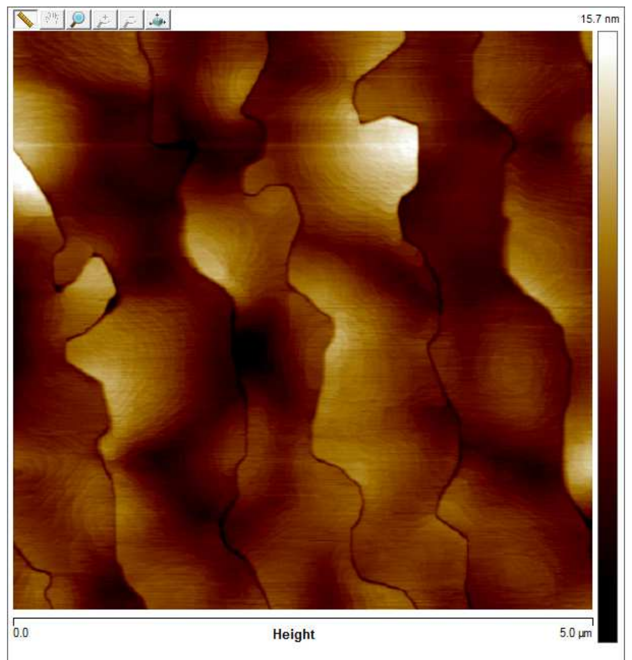
(002) Dark field TEM image in [110] cross section of the GaP/Si heterolayer. Self-annihilation of all antiphase domains leads to antiphase disorder free GaP layer after about 50 nm of overgrowth
B. Kunert et al. / Thin Solid Films 517 (2008) 140–143

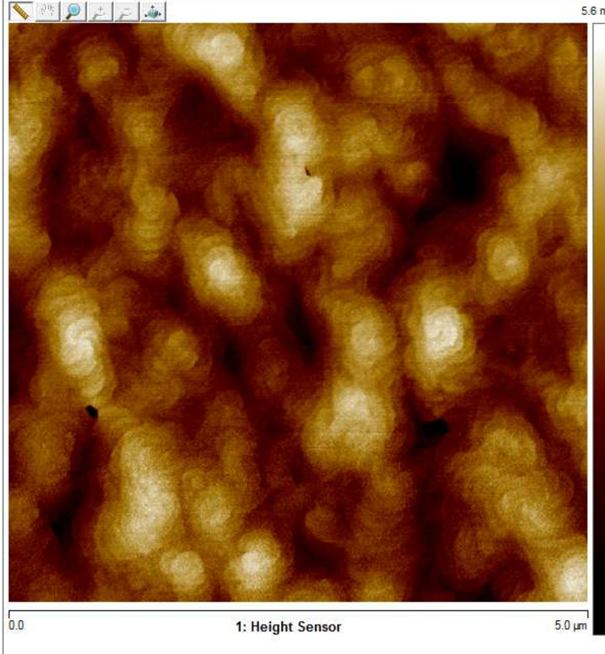
GaAs buffer growth on Si(100)

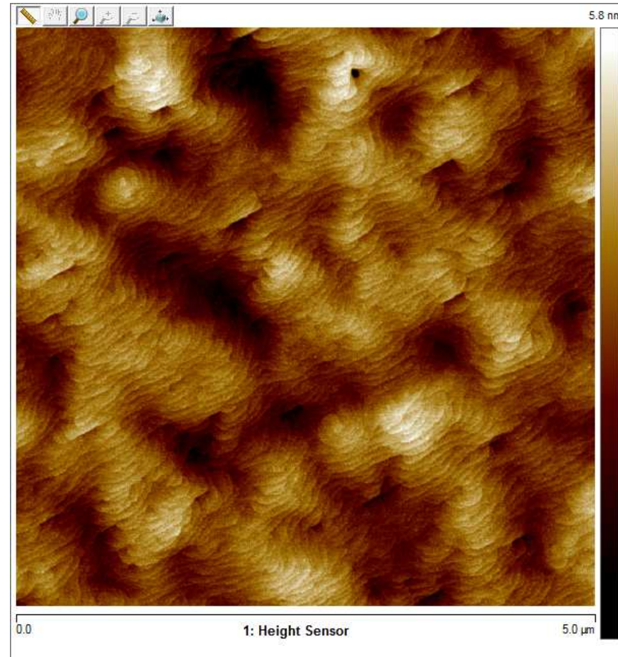
- Optimization of GaAs buffer on nominal Si(100)
- Growth of InP on GaAs/Si(100)
- Development of InGaAs growth on InP(100) substrates

GaAs/Si(100)

GaAs	Optimized GaAs	Optimized GaAs
RMS roughness : 1,4 nm	RMS roughness : 0,9 nm	RMS roughness : 0,8 nm
APB density = 1,83 µm^{-1}		

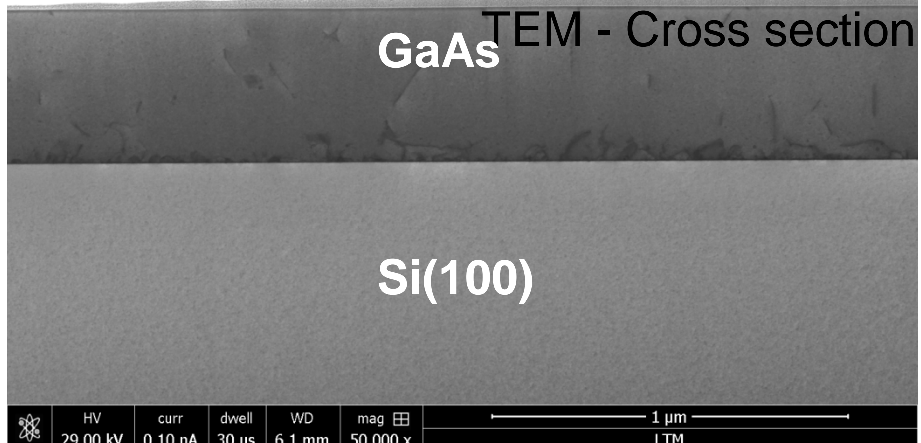


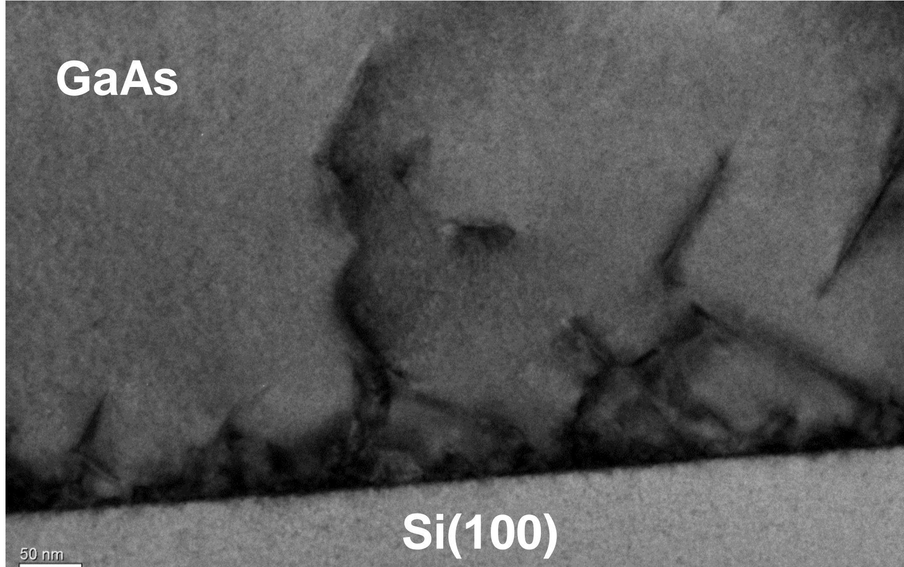




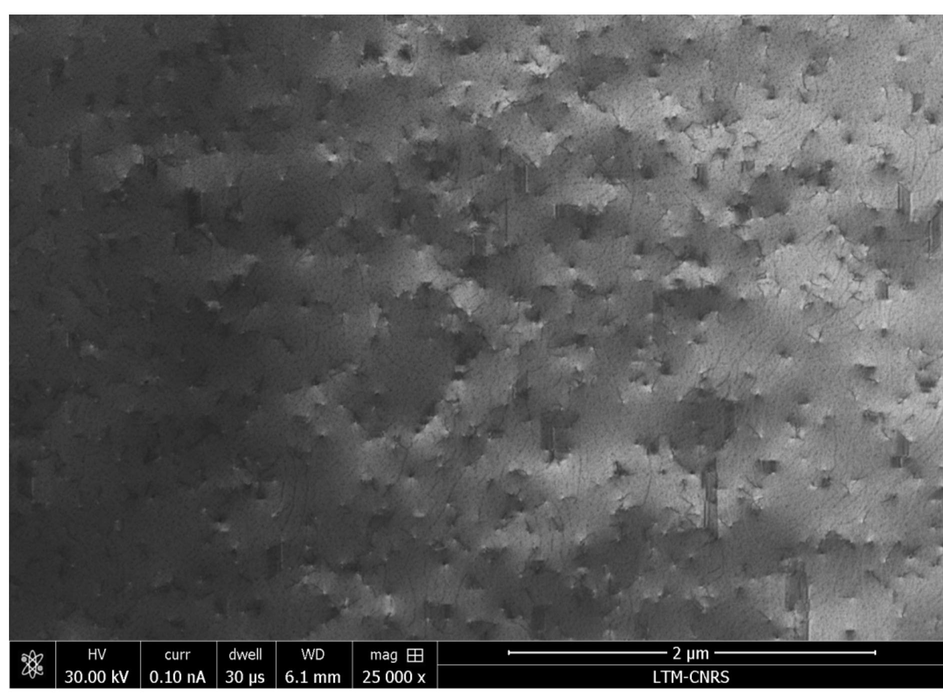
TEM analysis

TEM - Cross section





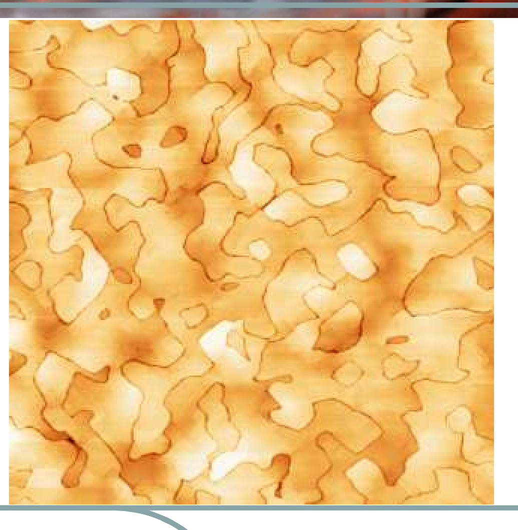
TEM – Top view

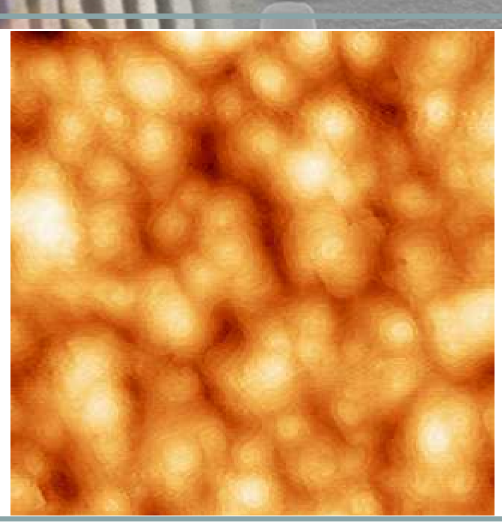


- Evaluation of dislocation density, 10^9 cm^{-2}

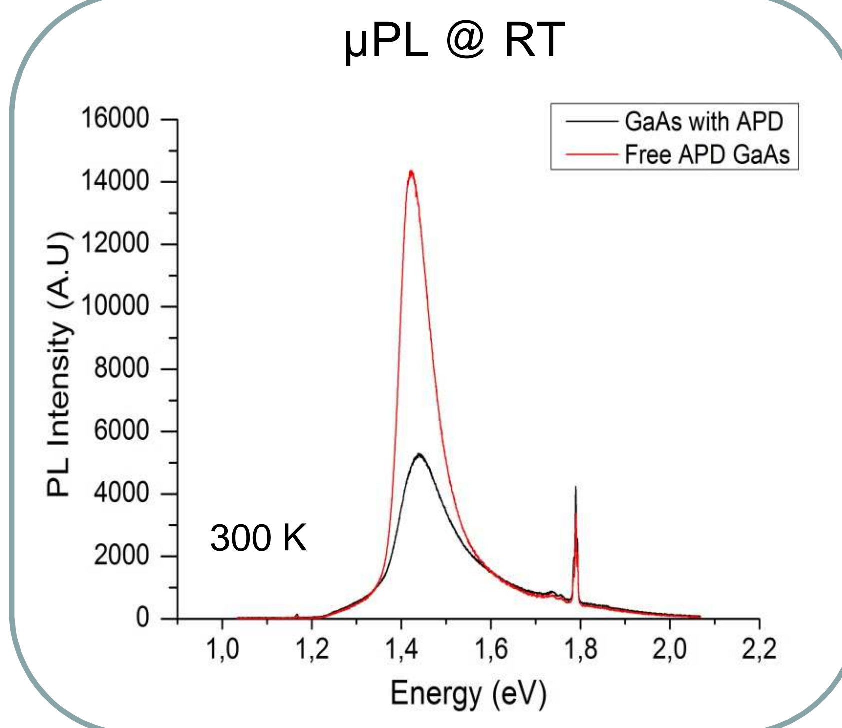
Physical properties of GaAs buffer layer

AFM 5x5 µm² pictures





µPL @ RT

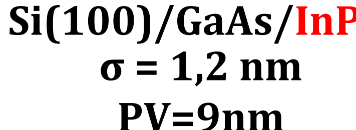


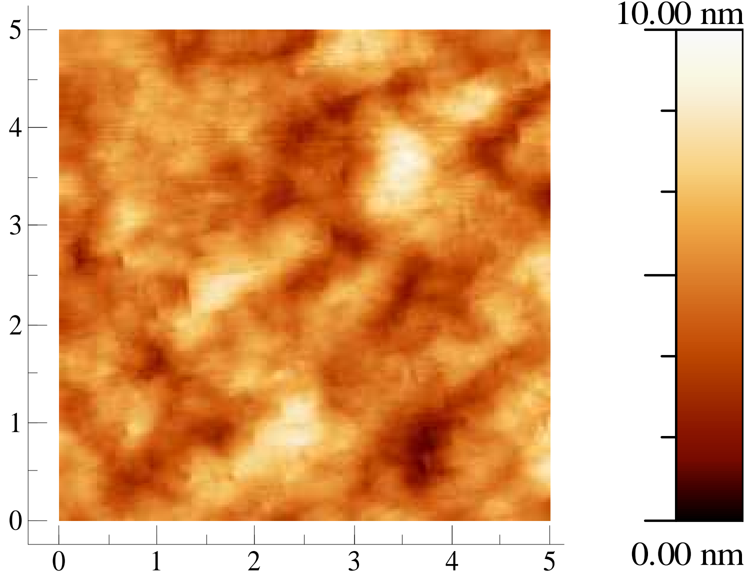
Hall effect measurements @ RT

	Roughness (nm)	APD density (cm^{-1})	µPL peak energy (eV)	FWMH meV	Electron mobility ($cm^2.V^{-1}.s^{-1}$)
GaAs with APD	1,7	4	1,44	140	200
Free APD GaAs	1	No APD	1,42	87	1600

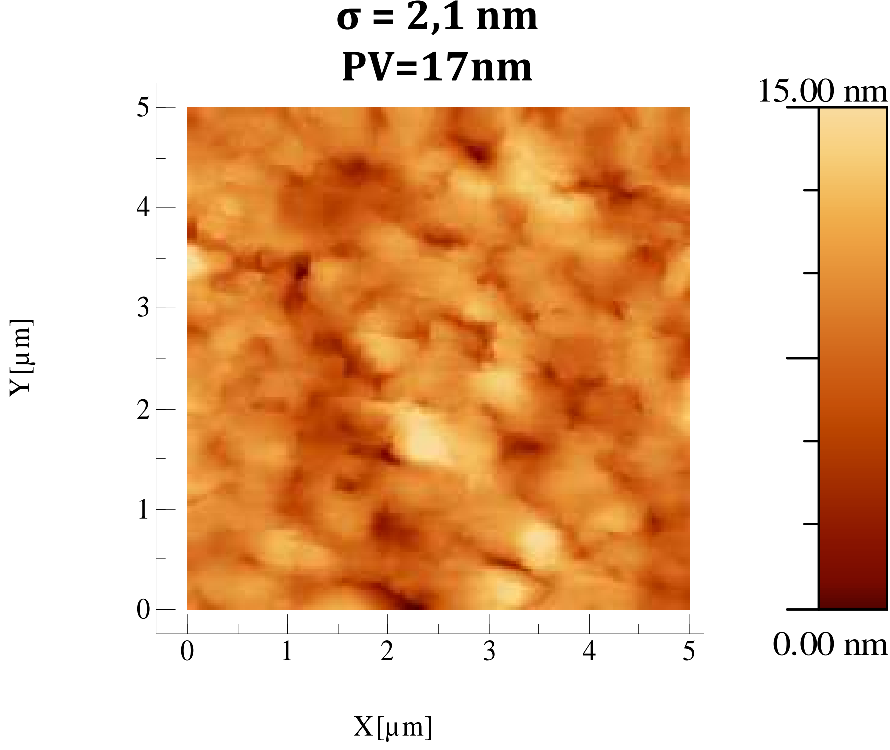
X8

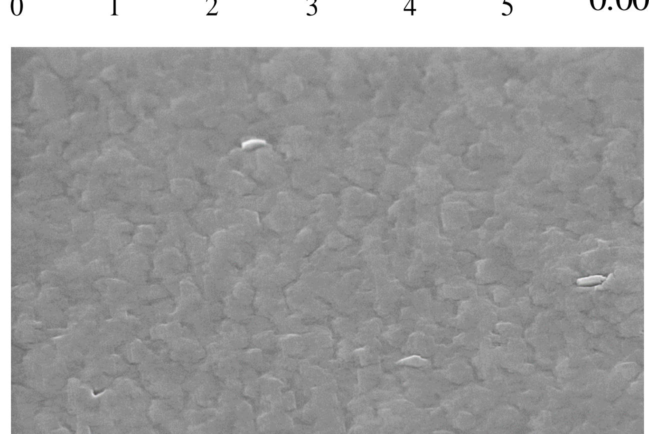
InGaAs/InP buffer/GaAs buffer/Si(100)





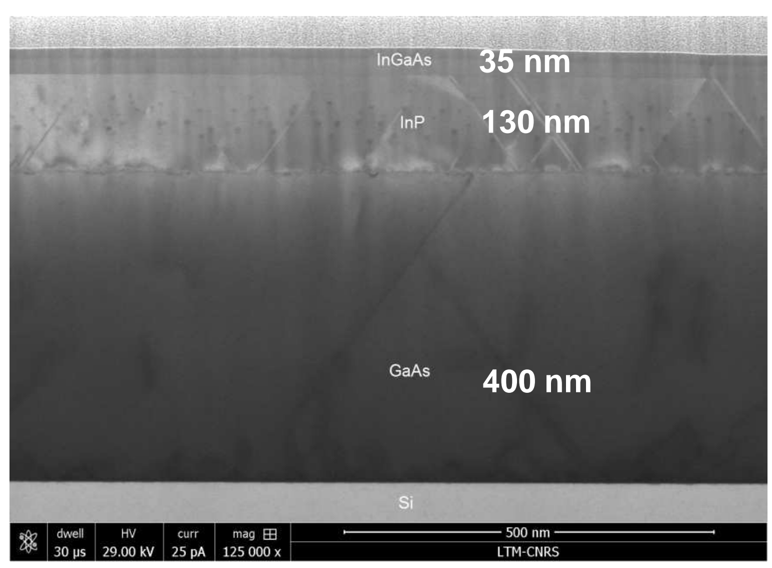
Si(100)/GaAs/InP/$In_{0,53}Ga_{0,47}As$

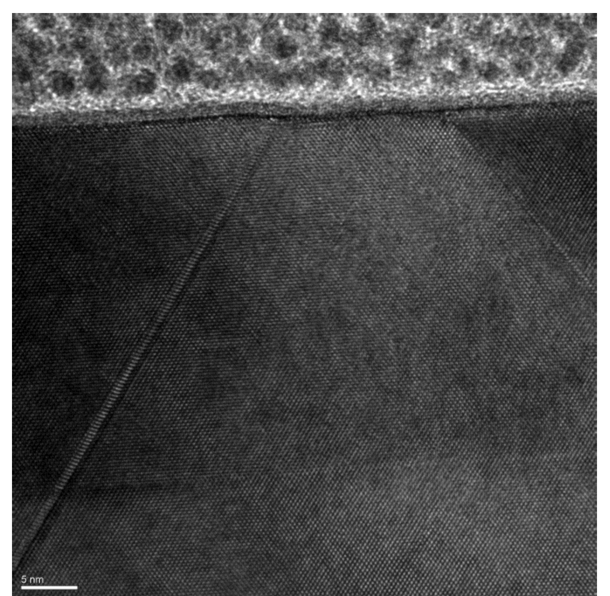


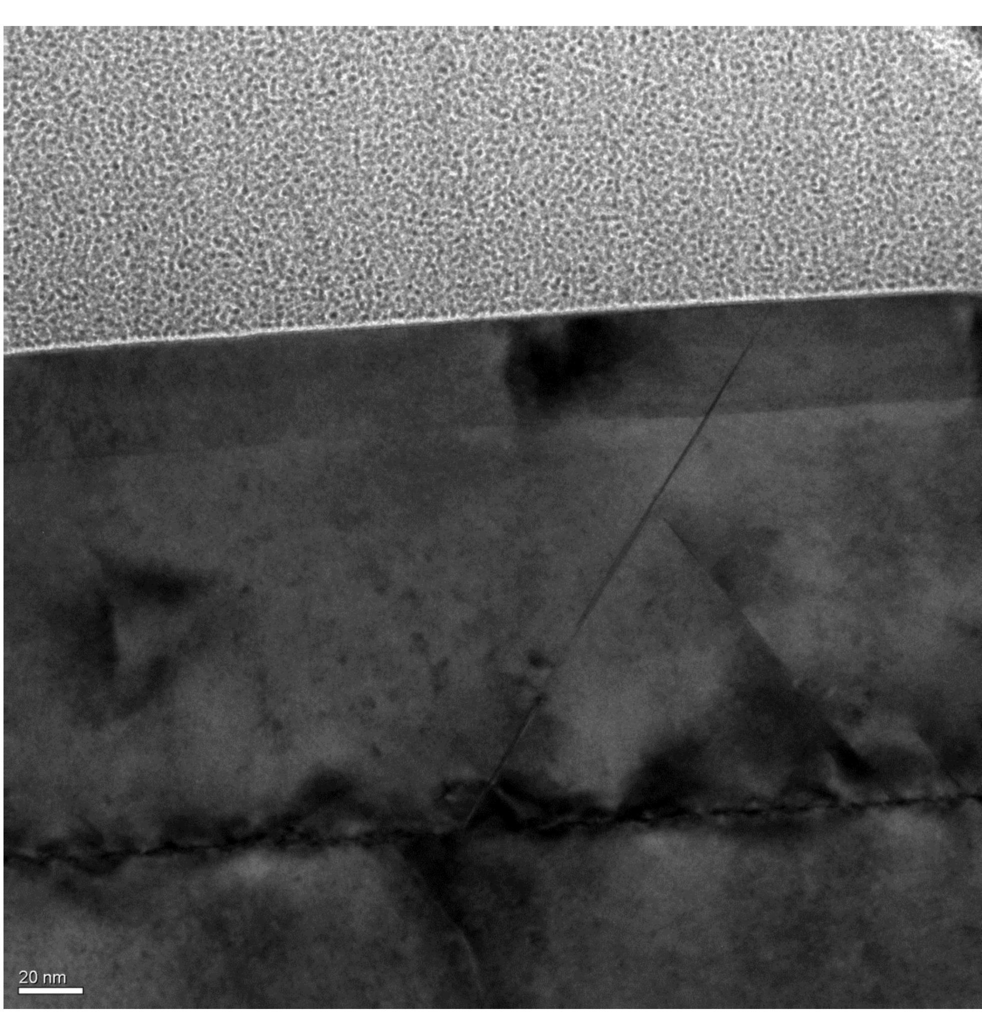


- Optimization of InGaAs still needed

STEM/TEM characterisation

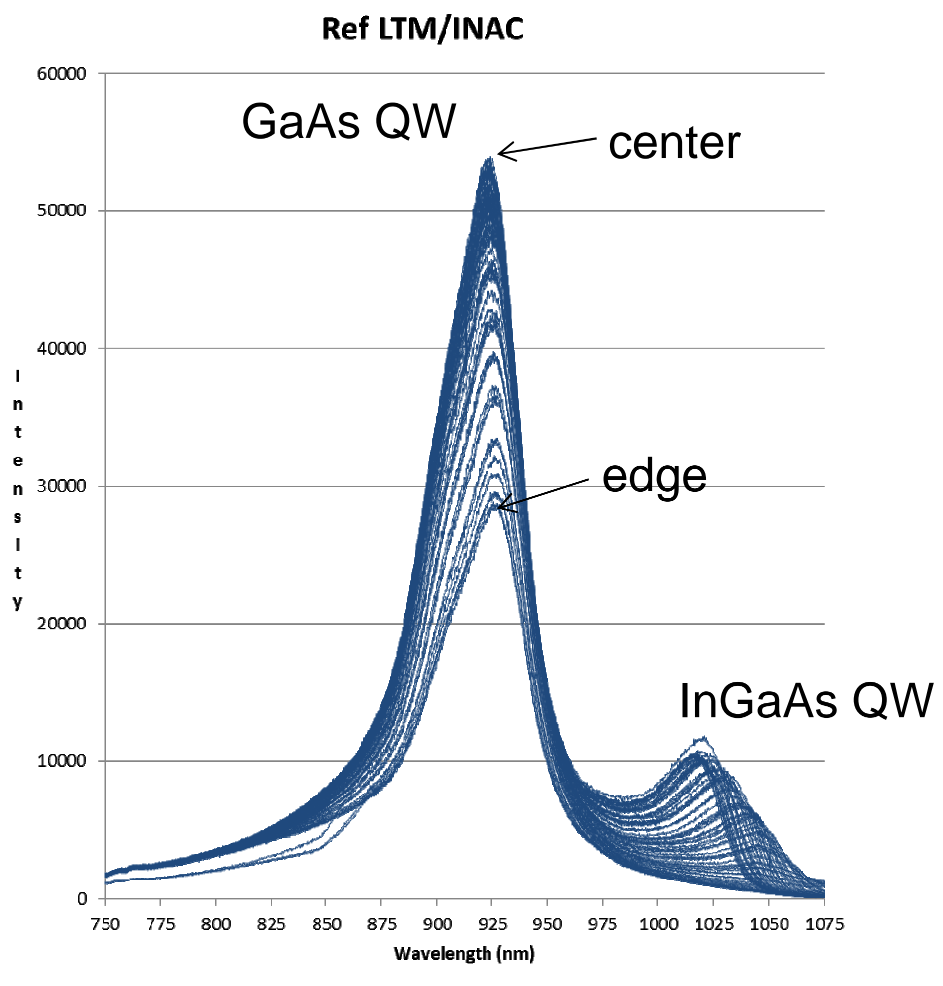






µPL at room temperature

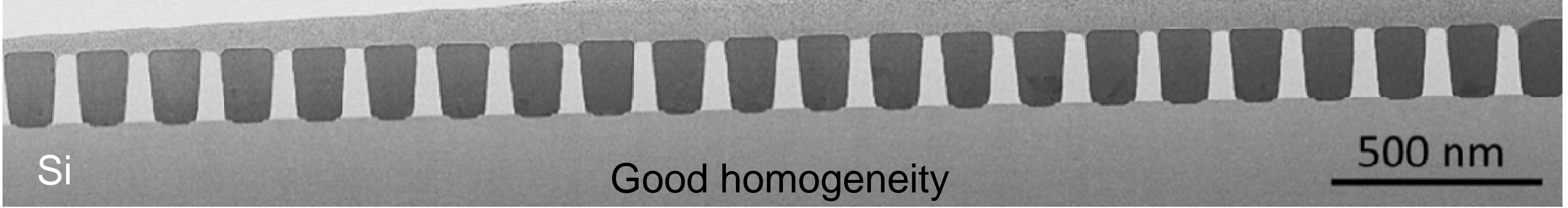
- GaAs/AlAs/**GaAs QW**/AlAs/GaAs/**InGaAs QW**/GaAs/AlAs/GaAs/Si(100)

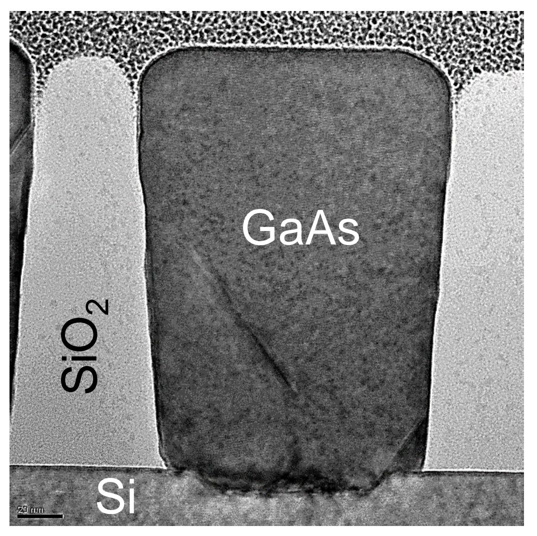


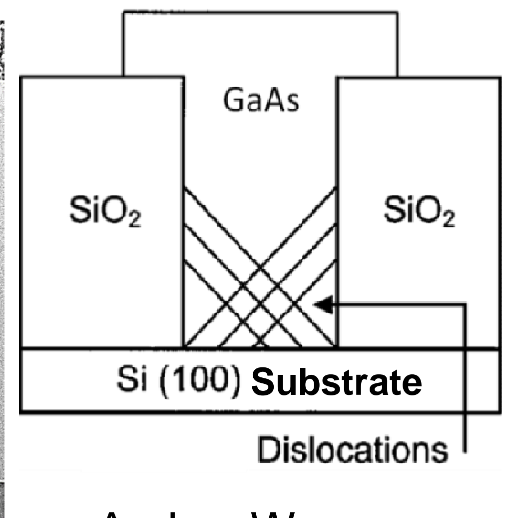
- High dislocation density (10^9 cm^{-2}), to be improved

Aspect Ratio Trapping : selective epitaxial growth

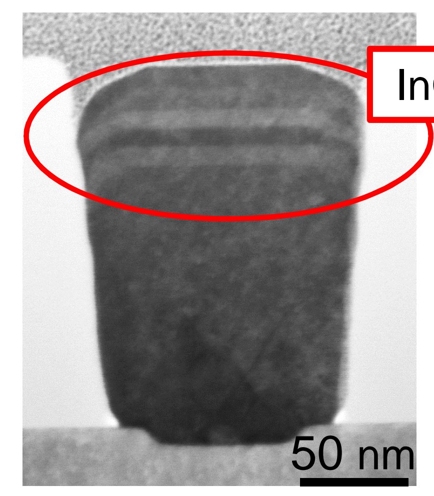
GaAs selective epitaxial growth in SiO_2 patterns (STEM cross sectional views)







Amber Wave



To measure the material quality :

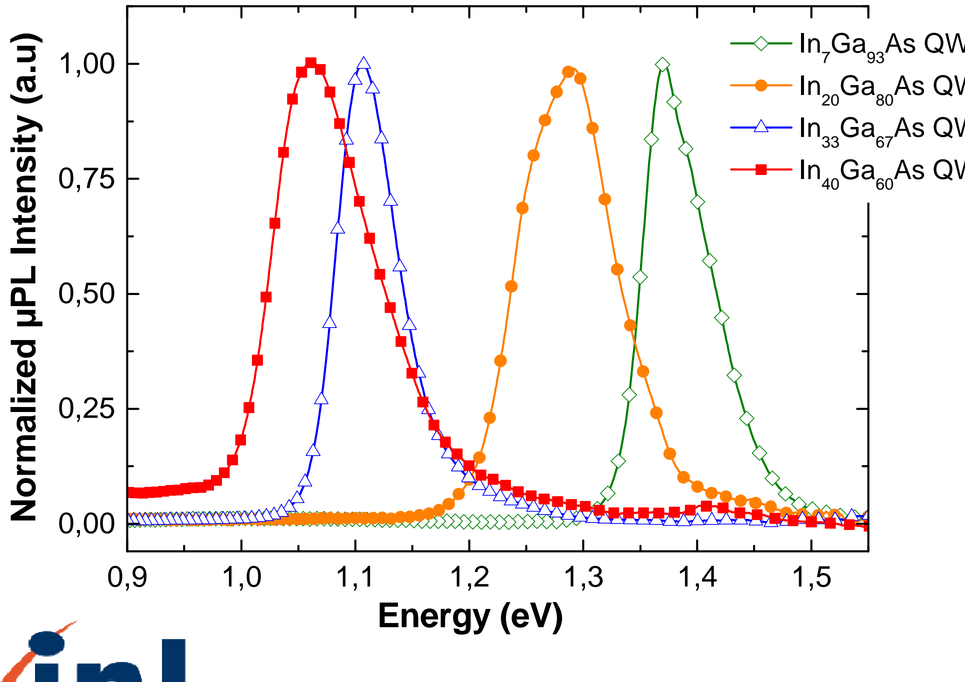
- Growth of InGaAs/AlGaAs quantum well in the top region : optical measurements

Annihilation of anti-phase boundaries, emerging dislocations, stacking fault

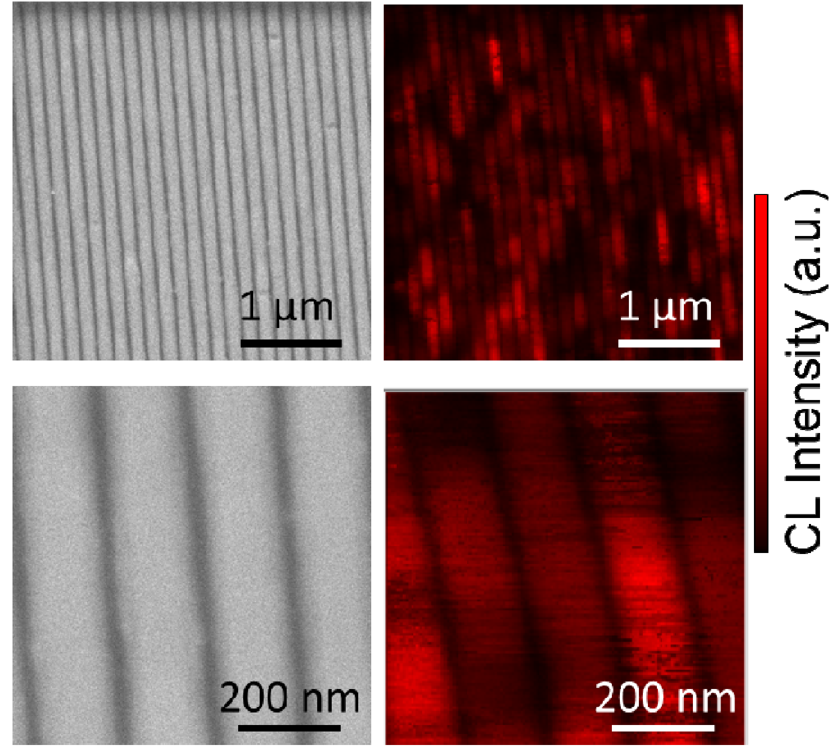
Optical measurements

R. Cipro et al., Appl. Phys. Lett. **104**, 262103 (2014)

- ❑ µPL at room temperature



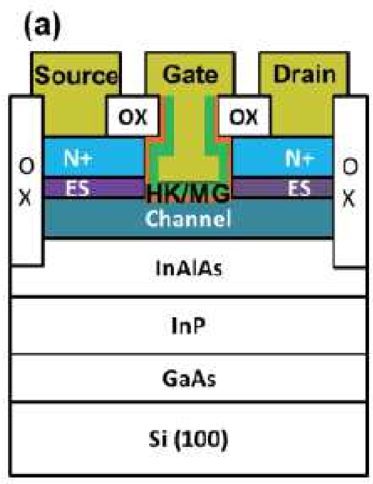
- ❑ Cathodolum. mapping at low temperature (top view)



inl

- ❑ **Room temperature µPL signal with FWHM of 60 meV is seen on pattern with dimension <200 nm**
- ❑ Non radiative recombination centers degrade the luminescence

InGaAs MOSFET on 300 mm wafers



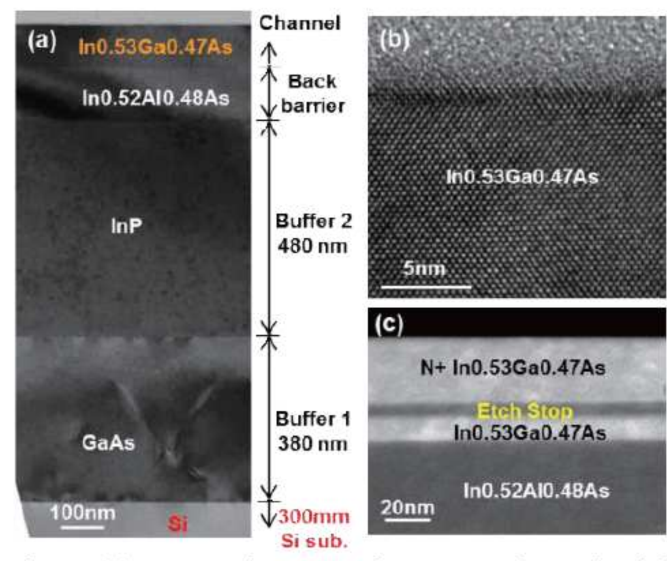


Fig. 1 (a) XTEM images of InGaAs channel with InAlAs barrier on Si. The metamorphic GaAs/InP buffer has thickness of ~0.86 μm, (b) HRTEM image of top InGaAs channel. (c) HAADF image of InGaAs device structure on GaAs/InP platform.

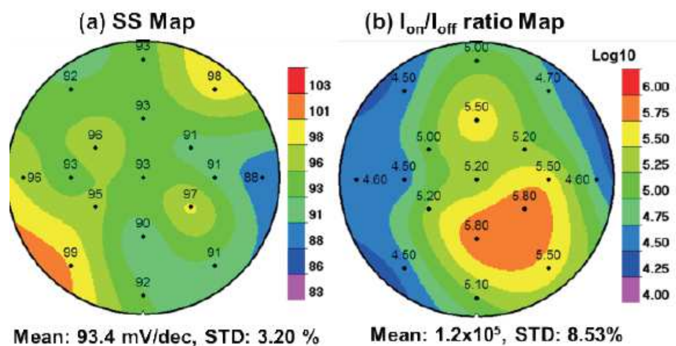


Fig. 8 The (a) SS and (b) I_{on}/I_{off} ratio map across 300mm wafer, respectively. The good uniformity with low SS(AVE) of 93 mV/dec and high I_{on}/I_{off}(AVE) ratio of 1.2×10^5.

M.L. Huang et al. , TSMC,
VLSI Symposium 2015

InAs/InGaSb/OI NMOS and PMOSFET

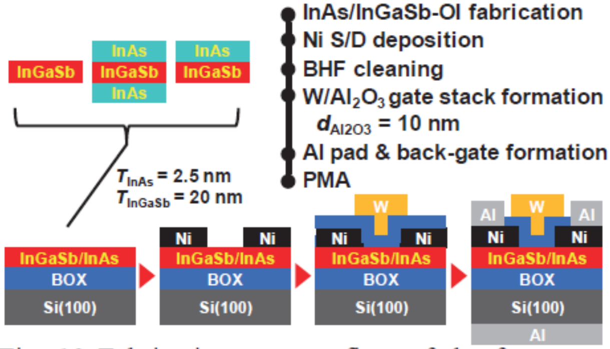


Fig. 10 Fabrication process flow of the front-gate InAs/InGaSb-OI CMOS on Si with single-layer InGaSb, InAs/InGaSb/InAs QW, and InAs/InGaSb hetero-channel.

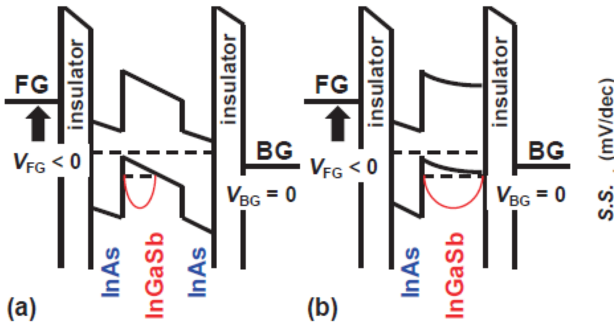


Fig. 15 Band diagram of the (a) QW and (b) hetero channel InGaSb-OI under $V_{FG} < 0$ and $V_{BG} = 0V$.

Fi
In
as

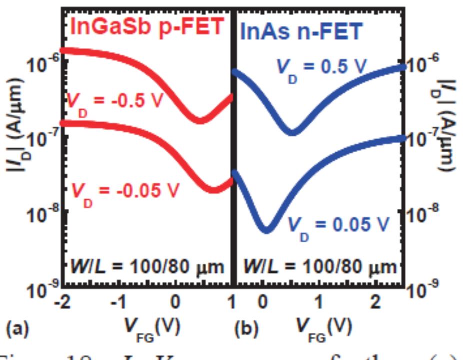


Fig. 18 I_D-V_G curves of the (a) InGaSb-OI p-MOSFET and (b) the InAs-OI n-MOSFET.

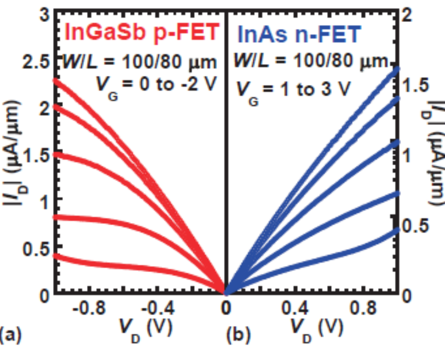


Fig. 19 I_D-V_D curves of the (a) InGaSb-OI p-MOSFET and (b) the InAs-OI n-MOSFET.

K. Nishi, et al. University of Tokyo, VLSI Symposium 2015

InGaAs-OI FinFET by selective + lateral epitaxy

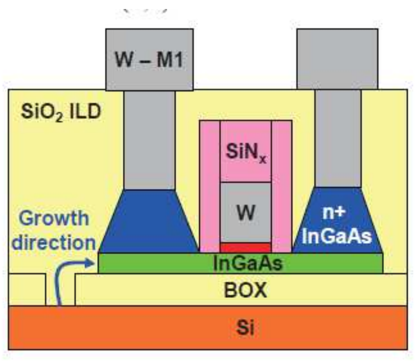


Fig. 8: Schematic of the fabricated gate-first InGaAs MOSFETs highlighting the InGaAs growth direction from the Si seed.

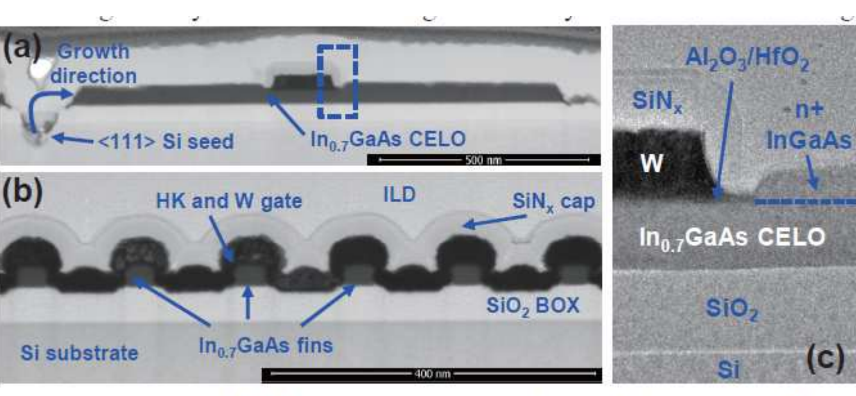


Fig. 9: Cross-sectional TEM images of a self-aligned InGaAs-OI FinFET integrated on Si by CELO. Views are (a,c) across the gate and (b) across the 25nm x 35nm fins. Standard gate-first process [8] with raised source/drain could be applied seamlessly thanks to the excellent InGaAs thermal stability.

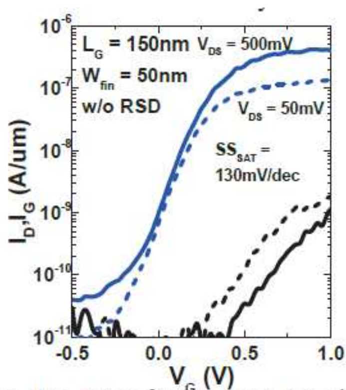


Fig. 10: Transfer an InGaAs FinFET without RSD showing an excellent I_{ON}/I_{OFF} ratio above 10^4 decades suggesting a low background doping.

L. Czornomaz, et al. IBM Zurich, VLSI Symposium 2015

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